PROFESSIONAL COMPONENTS

NDBOOK

Solid State Image Sensors and Peripheral Integrated Circuits

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Solid State Image Sensors and Peripheral Integrated Circuits

SOLID-STATE IMAGE SENSORS AND THEIR PERIPHERAL DRIVING AND VIDEO PROCESSING ICs

Philips Solid-State Image Sensors (SSIS) are the result of 10 years of dedicated research into electronic imaging. These highly advanced products are suitable for many consumer and professional applications.

This booklet contains data sheets covering the image sensor family and their drive and video processing ICs.

1. Sensors

The image sensor family consisting of the NXA1011, NXA1021, NXA1031 and the NXA1041, caters for monochrome, colour, 525 and 625 line applications. The sensors are particularly suitable for machine vision, optical character recognition, CCTV, ENG, and for use in the general medical field. A choice of picture quality grades are offered in order to achieve optimum cost/performance figures in any application.

2. Driving ICs

The TDA4301, TDA4302, TDA4305 and SAD1019 provide the drive and all the signals necessary for horizontal and vertical image transport. These ICs, combined with the SAA1043 sync generator, form the complete logic section of a sensor camera. Using this IC set, all of todays TV standards are provided for.

3. Video processing ICs

The TDA2501, TDA4303 and TDA4306 provide most of the video functions required by monochrome and colour cameras. These functions include amplification, γ correction, white clipping and contour correction etc. Together with other IC's the set can also provide full SECAM possibilities.

Solid-State Image Sensors

FRAME TRANSFER SENSOR

GENERAL DESCRIPTION

The NXA1011 frame transfer sensor is a solid state imaging device which produces two interlaced 294-line fields (including 6 lines for dark reference and testing) with an aspect ratio of 4:3.
The device is compatible with CCIR TV standards and has a 7,5 mm image diagonal matching the half-inch camera tube format. The NXA1011 sensor can be supplied without glass window upon consultation.

APPLICATIONS

- ENG cameras – the high blue sensitivity and good horizontal resolution makes this sensor suitable for 3-chip ENG colour cameras
- Surveillance cameras – solid state reliability, high resolution and sensitivity provide the quality to be an ideal successor for the Newvicon® or Ultricon® pick-up element
- Character and pattern recognition – the excellent linearity and uniformity recommends this sensor as a first choice for these applications
- Robotics – the small size, light-weight and mechanical ruggedness makes this sensor extremely suitable for all types of high resolution robot-vision applications
- Visual aids – the low voltage and mechanical ruggedness of this device allows design of safe and reliable cameras for visual aids

FEATURES

- Effective number of elements:
  604 (horizontal) x 576 (vertical)
- Dark reference: 1 line per field for black clamping
- 100 x anti-blooming margin
- Gamma is 1
- High sensitivity, low noise
- Freedom from lag, burn-in, geometrical distortion and microphonic noise

DEVICE ORGANIZATION

- Frame transfer charge coupled device
- Unit cell size: 10 μm (horizontal) x 15,6 μm (vertical)
- Dummy elements: the first 5 elements of the 3 output registers are dummy elements
- On-chip high sensitivity output amplifier
- Image area: 6,0 mm (horizontal) x 4,5 mm (vertical)
- Chip size: 6,95 mm (horizontal) x 9,35 mm (vertical)

FUNCTIONAL DESCRIPTION

The special electrode arrangement allows 26% of the photosensitive element to be free of polysilicon. This facilitates easy penetration of the blue light into the element to provide good blue sensitivity.

The layout of the sensor is shown in Fig. 1.
It comprises 3 functional areas:

- a matrix of photosensitive elements and integration electrodes,
- a storage section,
- three BCCD read-out registers.

Figure 2 shows the transport process in the imaging and storage regions. At time t_0, the start of the first field read-out from the imaging region, ϕ_3 is low and the charge is concentrated beneath ϕ_4 to ϕ_2. At t_1, ϕ_4 goes low and the charge in each pixel concentrates beneath ϕ_1 and ϕ_2. At t_2, ϕ_3 goes high and the charge packets advance one gate electrode, spreading out beneath ϕ_1, ϕ_2 and the following electrode ϕ_3. In the next step, at t_3, ϕ_1 goes low compressing the charge packets beneath ϕ_2 and ϕ_3, and at t_4, ϕ_4 goes high allowing the charge packets again to advance one gate electrode. This process continues in both the imaging and storage regions until all the charge packets have transferred to the storage region.

The sensor in the integration mode is shown in Fig. 3. The first field is generated when phases ϕ_4, ϕ_1 and ϕ_2 are high and ϕ_3 is low, Fig. 3(a). ϕ_3 effectively forms a potential barrier separating the pixels in the first field. The charges generated by incident light then integrate beneath ϕ_4 and ϕ_2, centred on ϕ_1. So each pixel extends vertically over four gate electrodes.
The potential distribution of the second field, and hence its position relative to the first field is shown in Fig. 3(b). The second field is always displaced by two gate electrodes relative to the first field, with its charge patterns centred on ϕ_3, and with ϕ_1 forming the barrier between pixels, thus providing a perfectly interlaced frame structure.

CAUTION

The image sensor is a MOS device which can be destroyed by static charging of the gates. Always store the device with short-circuiting clamps or on conductive foam plastic. When cleaning the glass window only use alcohol or acetone. Rub the window carefully and slowly. Dry rubbing of the window may cause static charges which can destroy the device.

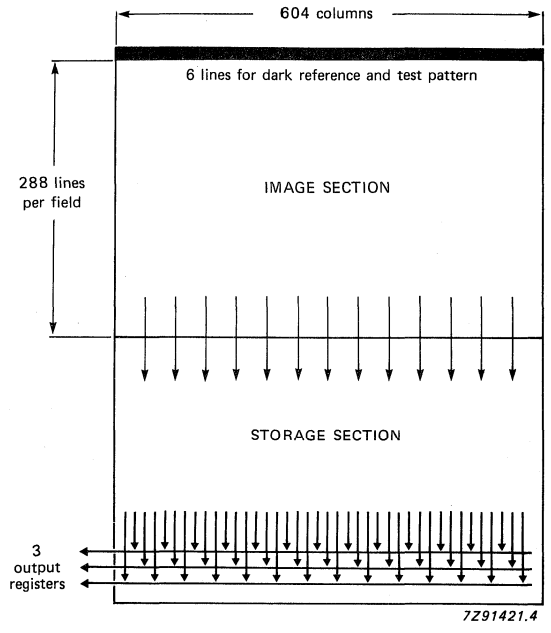


Fig. 1 Sensor layout and charge transport direction.

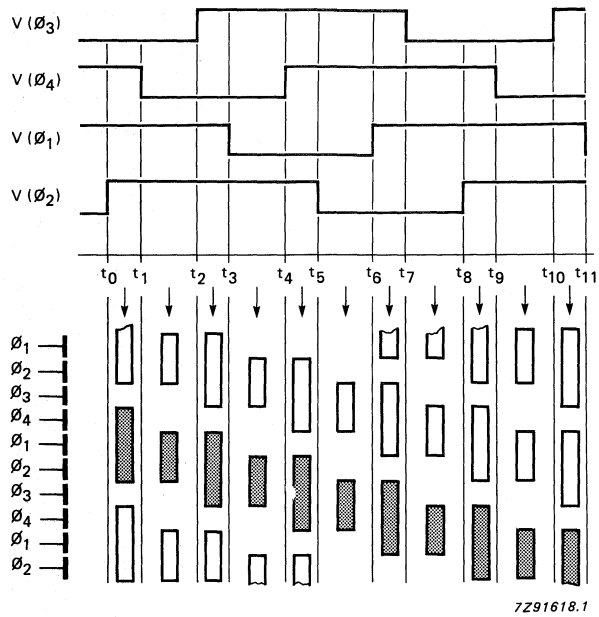


Fig. 2 Charge transport in the vertical direction.

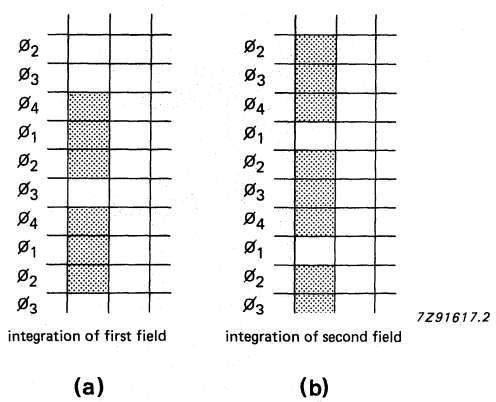


Fig. 3 Interlacing of the sensor.

(a) For integration of the first field, ϕ_4 to ϕ_2 are high, ϕ_3 is low forming a barrier between charge packets.

(b) For integration of the second field, ϕ_2 to ϕ_4 are high, ϕ_1 is low.

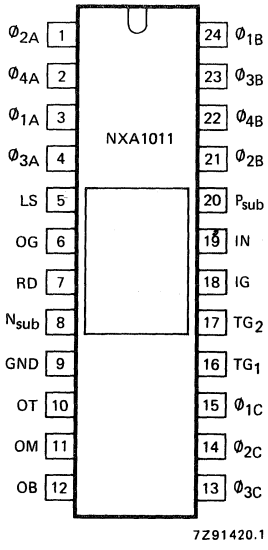


Fig. 4 Pin configuration.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	ϕ_{2A}	Vertical transfer clocks for image part
2	ϕ_{4A}	
3	ϕ_{1A}	
4	ϕ_{3A}	
5	LS	Light shield (Al. cover on storage part)
6	OG	Output gate
7	RD	Drain reset transistor
8	N_{sub}	N-substrate; supply voltage
9	GND	Ground
10	OT	Output top
11	OM	Output middle
12	OB	Output bottom
13	ϕ_{3C}	Horizontal transfer clock for output register
14	ϕ_{2C}	
15	ϕ_{1C}	
16	TG1	Transfer gates
17	TG2	
18	IG	Input gate (test point for manufacturing)
19	IN	Input diffusion (test point for manufacturing)
20	P_{sub}	P-substrate
21	ϕ_{2B}	Vertical transfer for storage part
22	ϕ_{4B}	
23	ϕ_{3B}	
24	ϕ_{1B}	

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Voltages with respect to P_{sub}				
RD	$V_{RD-PSUB}$	−0,5	+25	V
IN	$V_{IN-PSUB}$	−0,5	+25	V
Voltages with respect to N_{sub}				
RD	$V_{RD-NSUB}$	−10	+0,5	V
IN	$V_{IN-NSUB}$	−10	+0,5	V
all other connections		−25	+0,5	V
Current from one output		−	10	mA
Storage temperature range	T_{stg}	−55	+80	°C
Operating ambient temperature range	T_{amb}	−40	+60	°C

DC CHARACTERISTICS at T_{amb} = 60 °C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Voltage at LS	V_{LS}	−	V_{Nsub}	−	V
Voltage at OG (note 1)	V_{OG}	4	−	7	V
Voltage at RD; current to sensor: $I < 1\ \mu A$	V_{RD}	15,5	16	16,5	V
Voltage at N_{sub}; $I < 10$ mA	V_{Nsub}	19,5	20	20,5	V
Voltage at IG	V_{IG}	−	GND	−	V
DC level of output voltage at OT, OM, OB (notes 2 and 3)	$V_{OT;\ OM;\ OB}$	6	−	15	V
Voltage at P_{sub}; (note 1) current from sensor: $I < 50\ \mu A$	V_{Psub}	2	−	5	V
Voltage at IN	V_{IN}	−	V_{Nsub}	−	V
Power dissipation	P	−	80	150	mW
Leakage current of gates	I_{l}	−	−	2.5	μA

Notes

1. These values must be adjusted to the optimum operating point within the given range.
2. Measured with output buffer. See Fig. 5.
3. See Fig. 16.

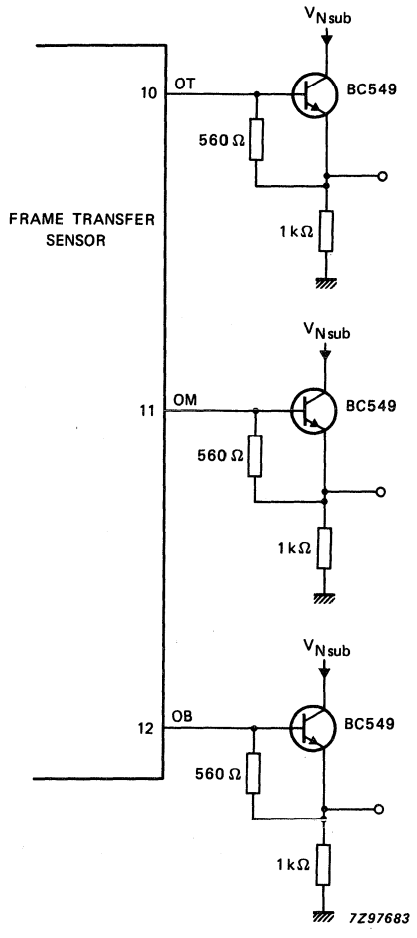


Fig. 5 Output buffer for measurements.

CLOCK CHARACTERISTICS (note 1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
LOW levels					
ϕnA, ϕnB	$V_{\phi nA/B}$	–	GND	–	–
ϕ1C, ϕ2C, ϕ3C ($\phi_{1CLOW} = \phi_{2CLOW} = \phi_{3CLOW}$) (note 2)	$V_{\phi nC}$	0	3,5	5	V
TG1 (note 2)	V_{TG1}	0	1	4	V
TG2 (note 2)	V_{TG2}	0	6,5	8	V
Amplitudes					
ϕnA, ϕnB, ϕnC	$V_{\phi(p-p)}$	9,75	10	10,25	V
Timing (see Figs 6 and 7)					
Horizontal clocks					
clock frequency (note 3)	f_c	–	3,85	–	MHz
rise time	t_{rc}	20	–	40	ns
fall time	t_{fc}	20	–	40	ns
overlap time	t_{ihc}	10	–	–	ns
	t_{ilc}	5	–	–	ns
Vertical clocks					
clock frequency	f_{cv}	–	625	–	kHz
rise time	t_{rv}	–	50	–	ns
fall time	t_{fv}	–	70	–	ns
overlap time	t_{ihv}	80	100	120	ns
	t_{ilv}	100	200	260	ns
Transfer gates					
rise time	t_{rTG}	–	70	–	ns
fall time	t_{fTG}	–	100	–	ns
Clock capacitance					
Each clock phase ϕnA, ϕnB	$C_{\phi nA/B}$	–	–	3000	pF
ϕnC, TG1, TG2	$C_{\phi nC}$, $C_{TG1/2}$	–	–	100	pF
Leakage current of the clock connections	I_l	–	–	2,5	μA

Notes

1. Measured with output buffer. See Fig. 5.
2. These values must be adjusted to the optimum operating point within the given range.
3. Deviations from this frequency result in incorrect aspect ratio.

ADJUSTMENT OF OPERATING LEVELS

For optimum performance, fine adjustment of the sensors DC levels is essential. When carrying out this operation the following points should be considered.

- Vertical stripes in the picture are usually the result of charges being unevenly sorted into the three output registers. This can be influenced by offsets $V_{\phi C}$, V_{TG1}, V_{TG2} and V_{OG}.
- The anti-blooming performance of a sensor is influenced by its internal vertical potential gradient. This can be optimized by adjusting V_{Psub}.

DRIVING PULSE WAVEFORMS

The specifications of the sensor are measured when the following clock pulses are applied (Figs 6 and 7). In principle the sensor can be operated with different clock pulses, e.g. different clock frequencies (overlap conditions have to be maintained).

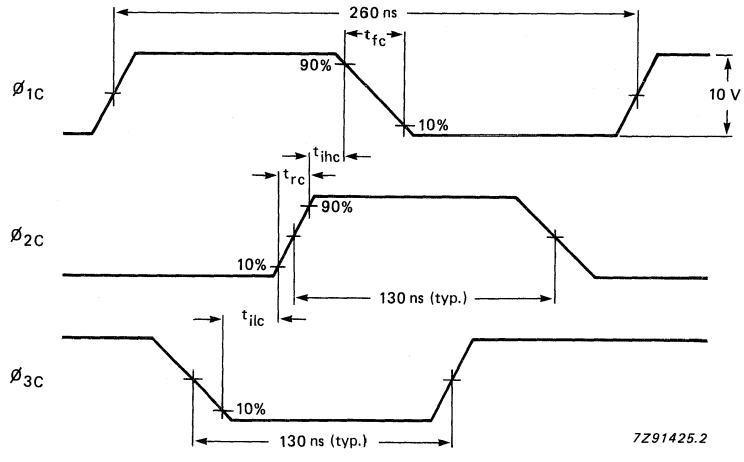


Fig. 6 Horizontal transport timing waveforms for the sensor electrodes (ϕ_{nC}); times measured at the 10% and 90% points of the amplitude.

DRIVING PULSE WAVEFORMS (continued)

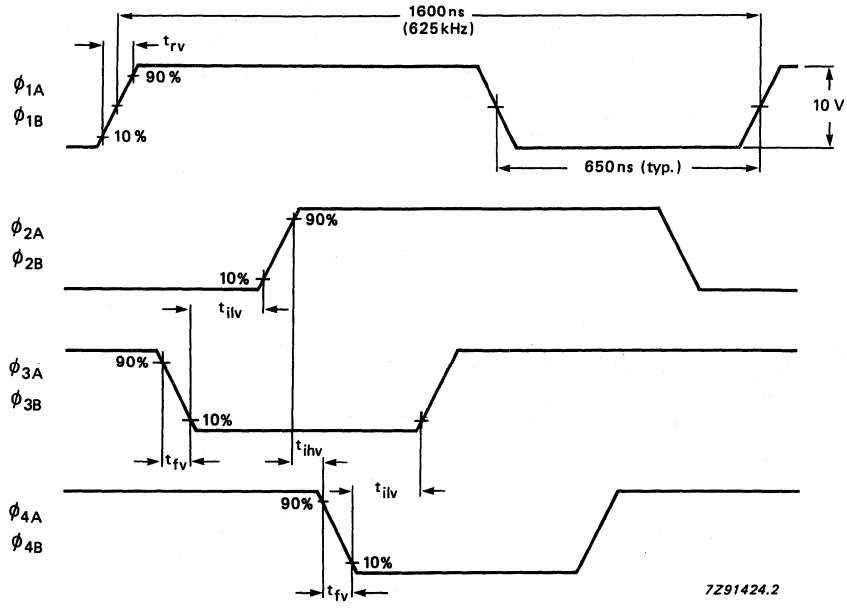


Fig. 7 Vertical transport timing waveforms for the sensor electrodes (ϕ_{nA}, ϕ_{nB}); times measured at the 10% and 90% points of the amplitude.

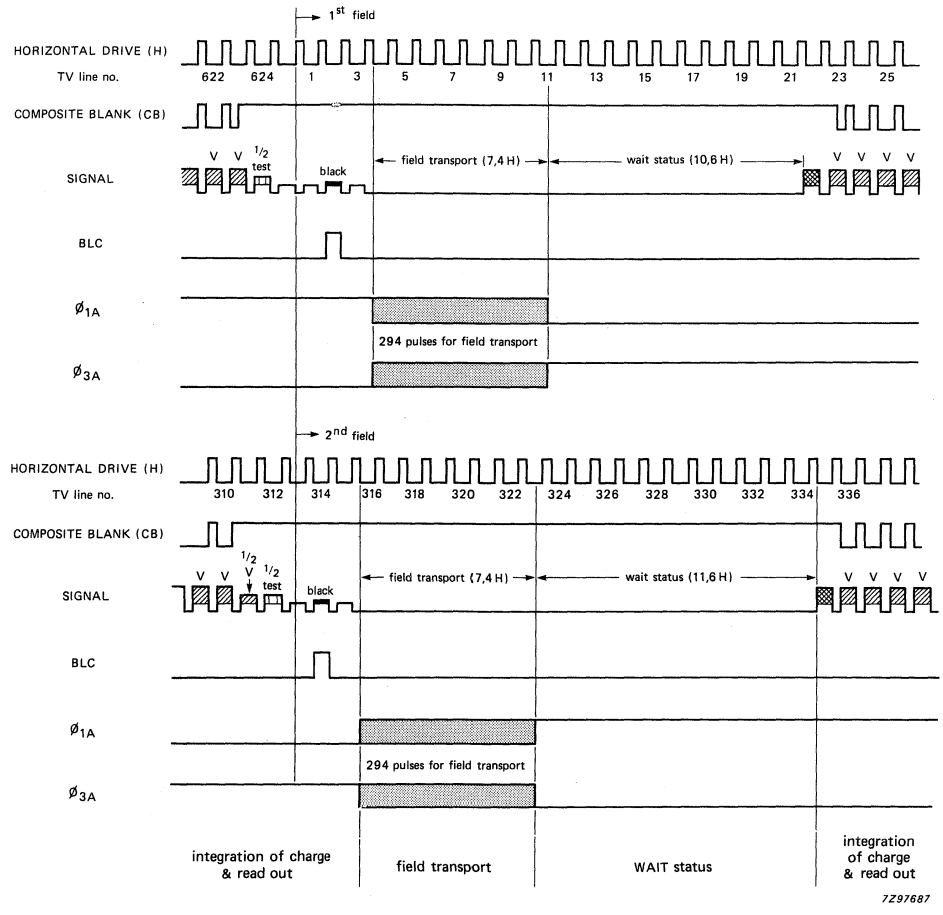


Fig. 8 Drive-pulse sequence and line numbering for field transport.

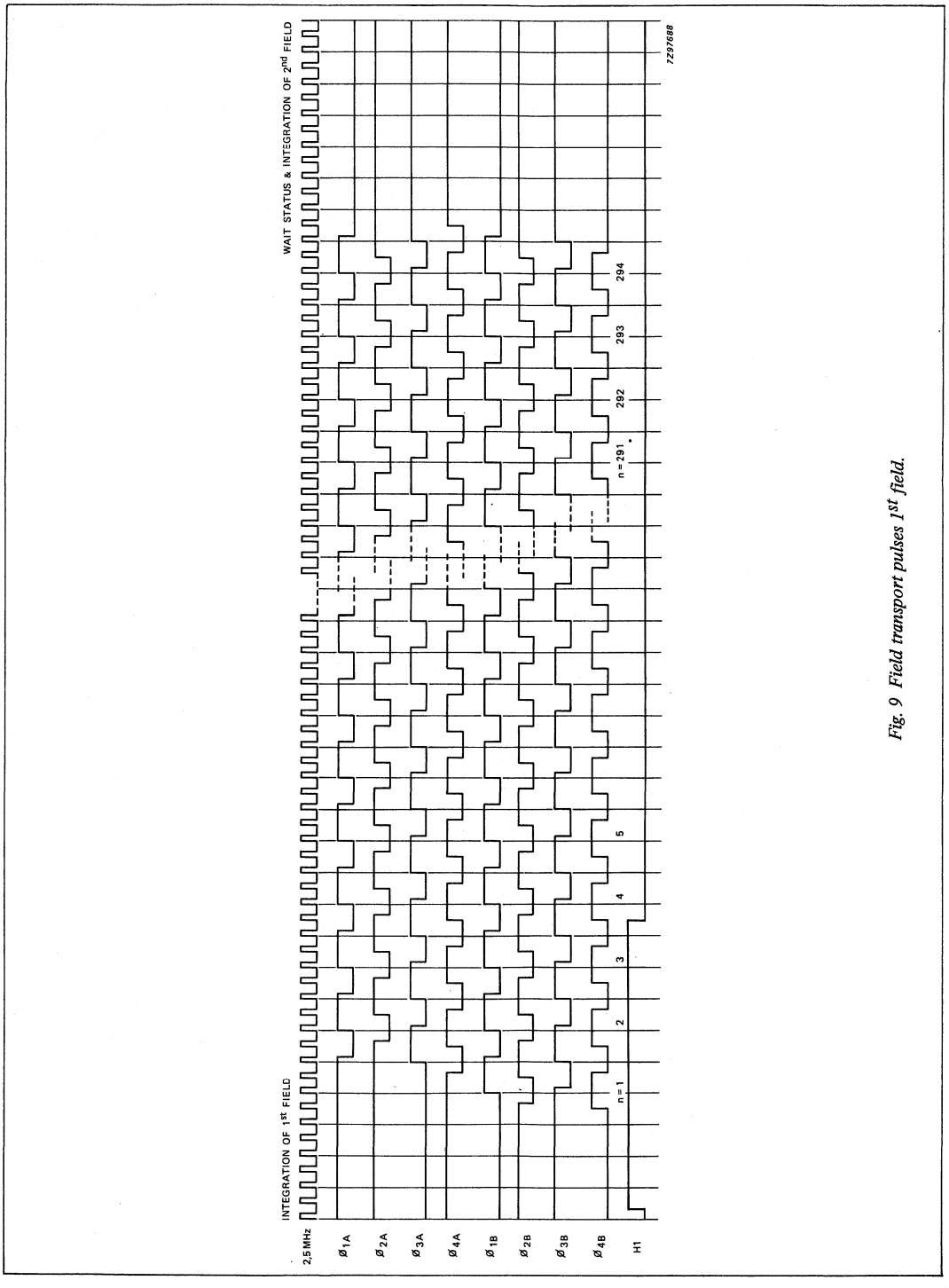


Fig. 9 Field transport pulses 1st field.

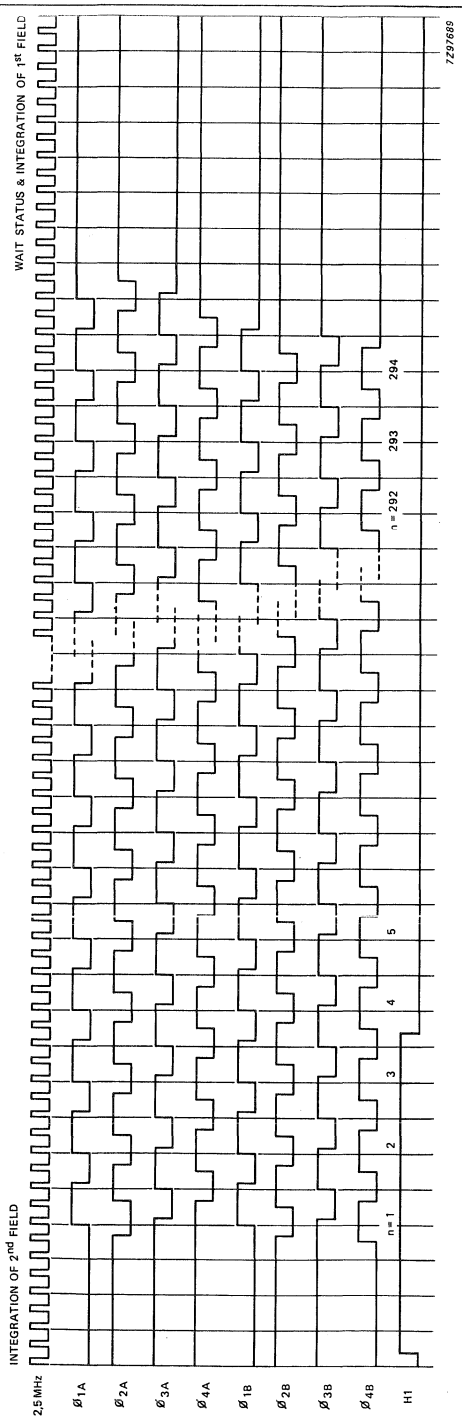


Fig. 10 Field transport pulses 2nd field.

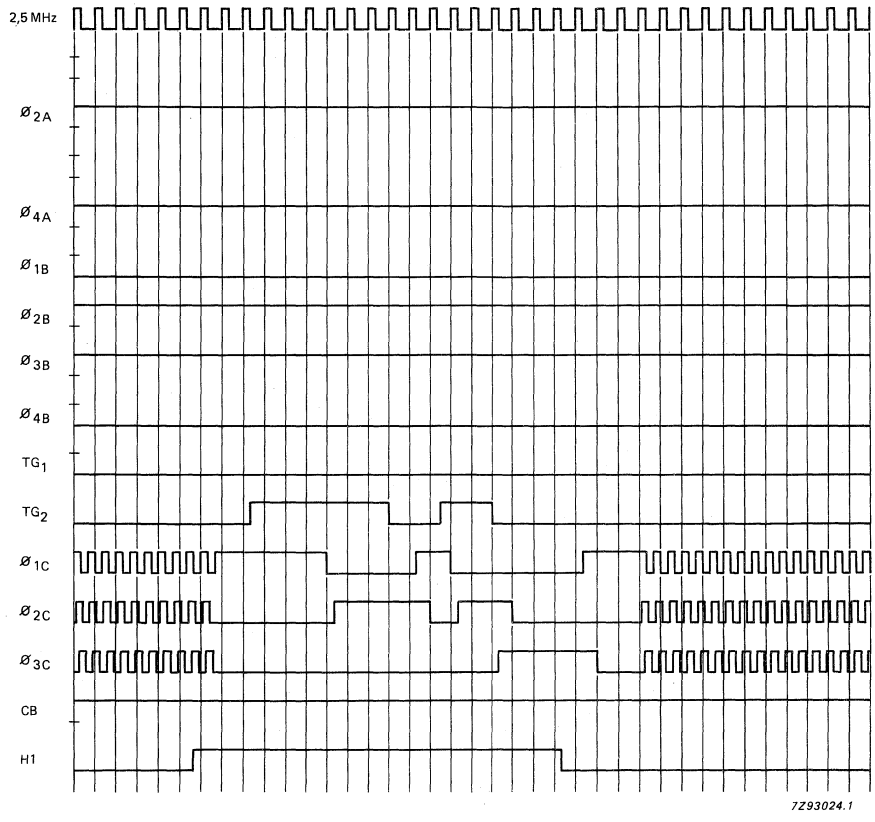


Fig. 11 Wait status.

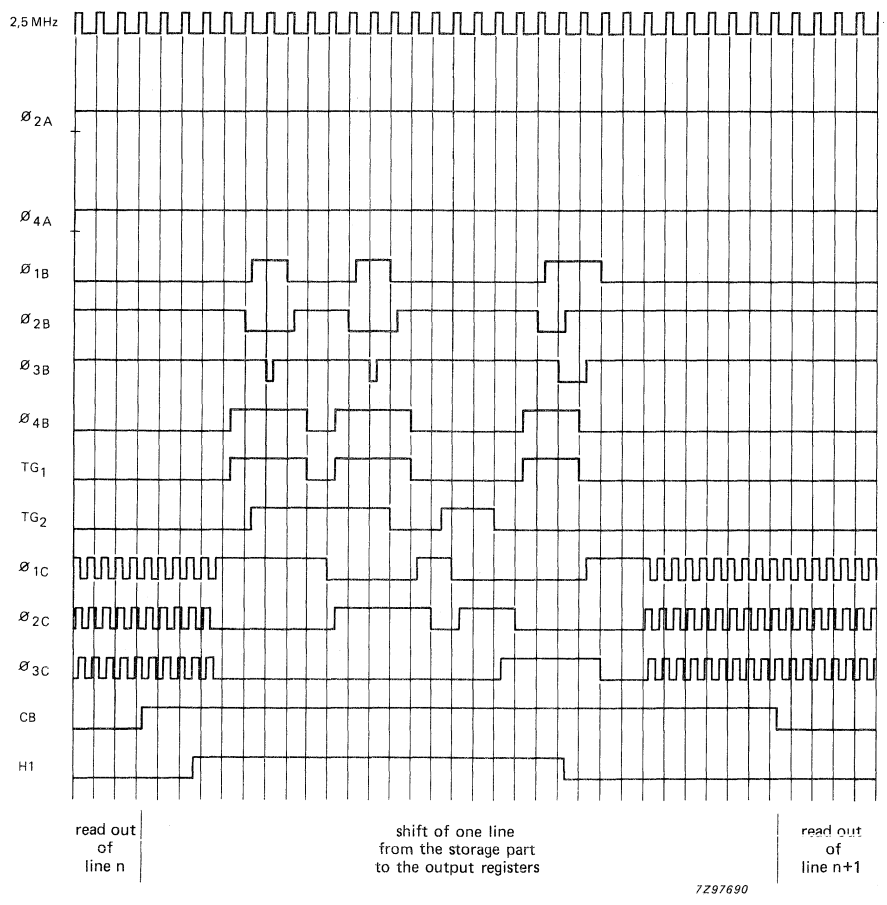


Fig. 12 Read out of the output registers and sorting of the signal into output registers.

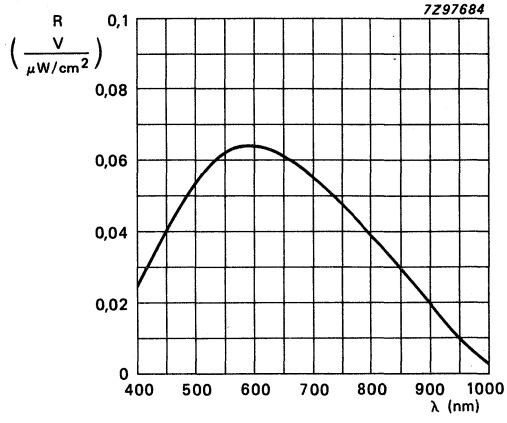


Fig. 13 Spectral response.

OUTPUT CHARACTERISTICS at T_{amb} = 60 °C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Load capacitance	C_L	–	–	10	pF
Output signal voltage at standard illumination (peak-to-peak value) (S/N typ. 50 dB) (notes 1 and 2)	V_{OTS} V_{OMS} V_{OBS}	70	100	–	mV
Signal to noise ratio at standard illumination (notes 1, 2 and 3)	S/N	–	50	–	dB
Output signal voltage at saturation (peak-to-peak value) (note 2)	V_{Osat}	300	600	1200	mV
Maximum illumination on the sensor without blooming (note 4)	E_B	2000	–	–	lx
Transport inefficiency					
horizontal one step	ϵ_H	–	–	$8{,}5 \times 10^{-5}$	
vertical one step	ϵ_V	–	–	5×10^{-5}	
Dark current	I_D	–	–	3	nA
Smear (note 5)					%

Notes

1. 5 Lx on the sensor, colour temperature of light source 3200 K, Hoya-IR-filter C500S, 1 mm is used.
2. Measured with output buffer.
3. 200 kHz to 5 MHz, weighted, T_{amb} = 25 °C
4. See 'Definition of blooming'.
5. See 'Definition of smear'.

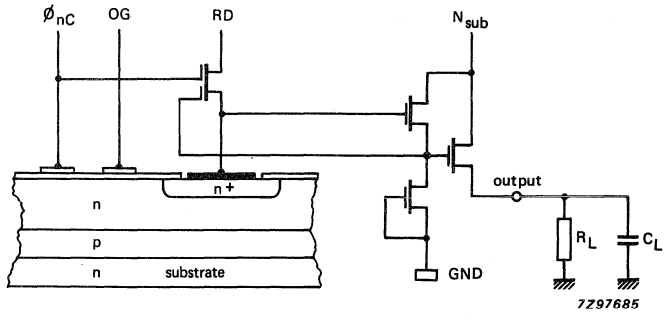


Fig. 14 Circuit diagram for one output channel.

DEFINITION OF SMEAR

During the field transport time the complete field is shifted over the image section. So each pixel of one column is illuminated by the light on all the other pixels of one column for a short time. Therefore a bright spot makes a bright vertical stripe on the image. This effect is called smear. The brightness of the stripe depends on the height of the spot and on the illumination of the spot.

It is defined by the equation:

$$V_{smear} = \frac{t_{field\ transport}}{t_{integration}} \times \frac{h}{H} \times \frac{E}{E_{sat}} \times V_{sat}$$

Where:

V_{smear} = Additional output voltage due to smear
$t_{field\ transport}$ = 0,47 ms
$t_{integration}$ = 19,5 ms
h = Height of bright spot
H = Height of the complete image
E = Illumination of the spot
E_{sat} = Saturation illumination
V_{sat} = Output voltage at saturation

Example:

Spot height is 10% of the height.
Spot illumination is 100% of saturation.

$$V_{smear} = \frac{0,47}{19,5} \times 0,1 \times 1 \times V_{sat} = 0,0024 \times V_{sat}$$

DEFINITION OF BLOOMING

When part of the image section (spot) is illuminated above saturation level and with the rest of the image dark, at a certain level of overexposure (2000 lx for the NXA1011), the area of the spot increases irregularly. This effect is called blooming.

PICTURE ELEMENT DEFECTS

picture quality at T_{amb} = 60 °C

GRADE	PIXEL DEFECTS (note 1)	CLUSTERS (note 2)	COLUMN DEFECTS (note 3)
01	0	0	0
02	2	0	0
03	10	2	0
04	35	5	2

Notes

1. A picture element is considered defect, if its signal deviates more than ±10% from the mean signal of the neighbouring picture element at standard illumination.
2. A cluster is a pair of two defect pixels at a distance of less than 3% of the picture height. The sum of pixel defects and clustered pixel defects does not exceed the number of permitted pixel defects. A pixel defect in the same place in odd and even fields is not defined as a cluster.
3. If more than two pixel defects occur in one column, this is considered a column defect. Additionally the indicated number of defect pixels is allowed.

OUTPUT SIGNAL

The output signal is a pulse sequence with a DC offset. The HIGH level of the output pulses, dependent upon the DC adjustments, varies between 6 and 15 volts. The LOW levels depend upon the signal voltage, itself a function of the intensity of the light falling on the sensor, and is between 1.0 and 0.2 volts below the HIGH level. These pulses contain the video information and need further processing to be converted into a signal suitable for use in standard video circuitry.

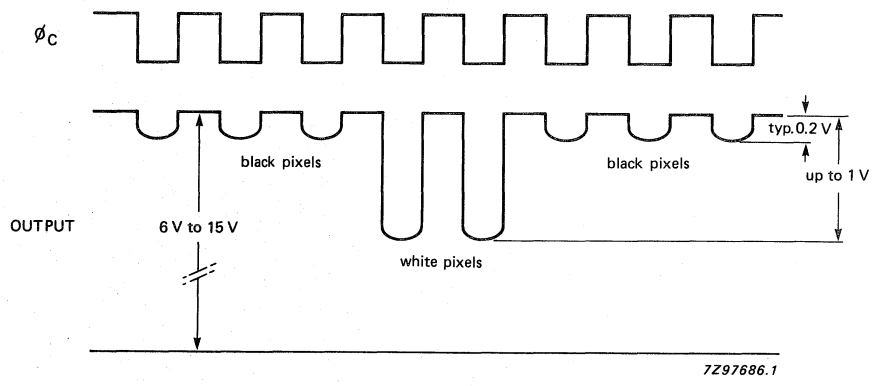


Fig. 15 Typical signal at the sensor output.

MECHANICAL PARAMETERS

The sensor is encapsulated in a 24-lead dual in-line ceramic package with a high-quality glass viewing window on the top side for admittance of light to the sensor.

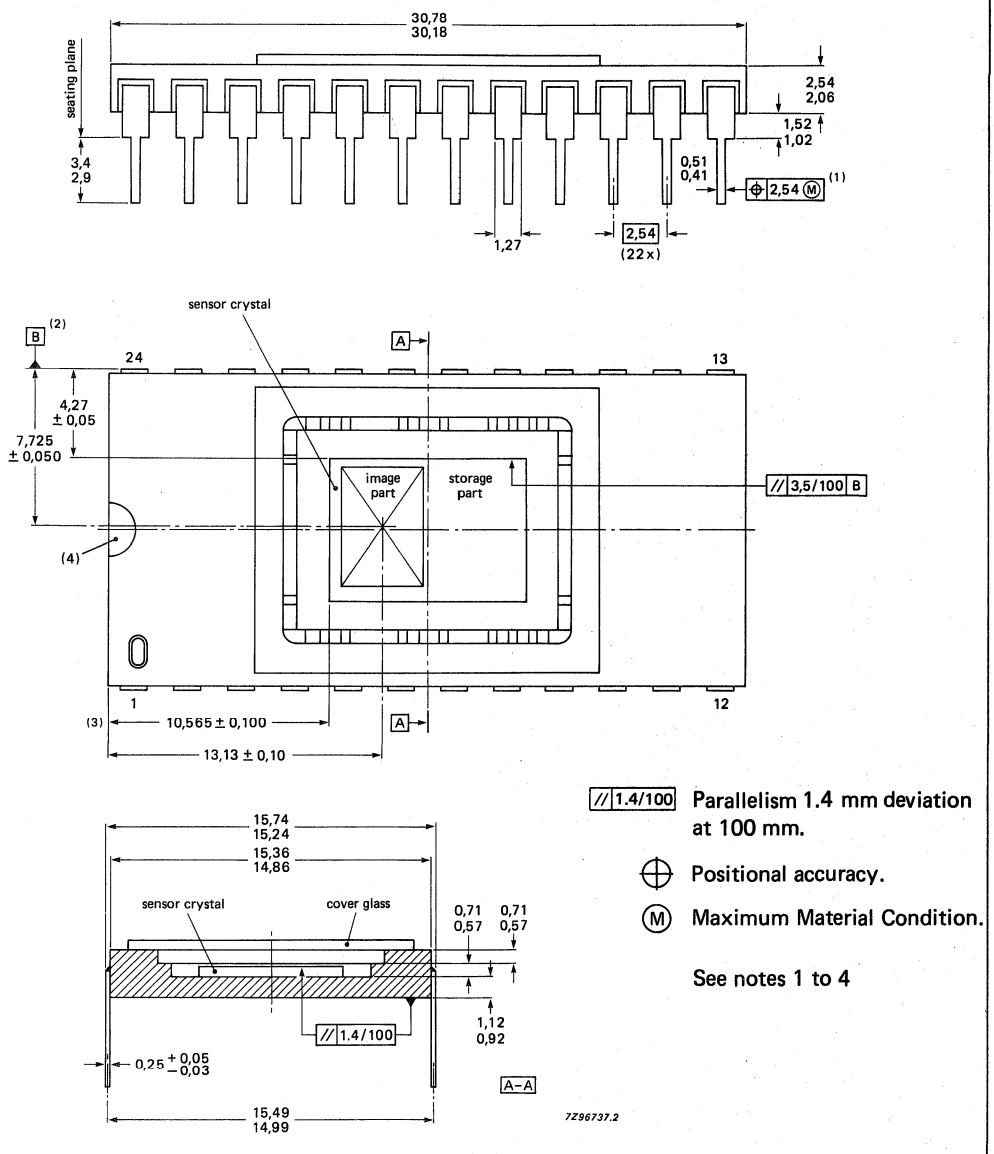


Fig. 16 Package outline; dimensions in mm (also see notes).

Notes to Fig. 16

1. Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.
2. Line B is the connection line between pins 13 and 24. Pins 14 to 23 are not necessarily exactly on this line.
3. These two dimensions are measured at the centre-line of the package.
4. The gold plateau is internally connected to N_{sub}.

GENERAL DIMENSIONS (See Fig. 16)

Chip thickness	525 ± 15 μm
Cover glass thickness	550 ± 50 μm
Thickness of glue layer between sensor and cavity bottom	80 ± 30 μm
Refractive index	1,5
Transmission (400-700 nm)	90%

Sensor is filled with nitrogen.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or Wave

The maximum permissable temperature of the solder is 260 °C, this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the seating plane but the temperature of the ceramic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

APPLICATION INFORMATION

Figure 17 shows a circuit for providing the pulse sequences needed to drive the sensor. A SAA1043 sync-pulse generator provides the three TV standards, namely PAL, SECAM and NTSC. These include vertical and horizontal blanking, and black-level clamping. It also provides other signals essential for tv camera operation and can be triggered externally for operation with, for example, a VCR or computer. The sync-pulse generator drives a SAD1019 multi-norm pulse-pattern generator (MNPPG) developed specifically for the image sensors. It provides all the clock signals except the pulses for the horizontal read-out registers. Its use avoids the need to develop complex circuitry for driving the NXA1011. Fast clock pulses for the three horizontal read-out registers are generated by a horizontal clock generator. The three 3.85 MHz pulse trains generated differ in phase by 120°. The output levels from the MNPPG are too low to drive the shift registers directly, therefore, additional vertical driver IC's (VDR) TDA4301 are required to boost these signals to suitable levels. During the horizontal blanking period, slow pulses derived from the MNPPG need to be applied to the horizontal registers to sort the charge packets into the three horizontal read out registers.

More detailed information is available on request.

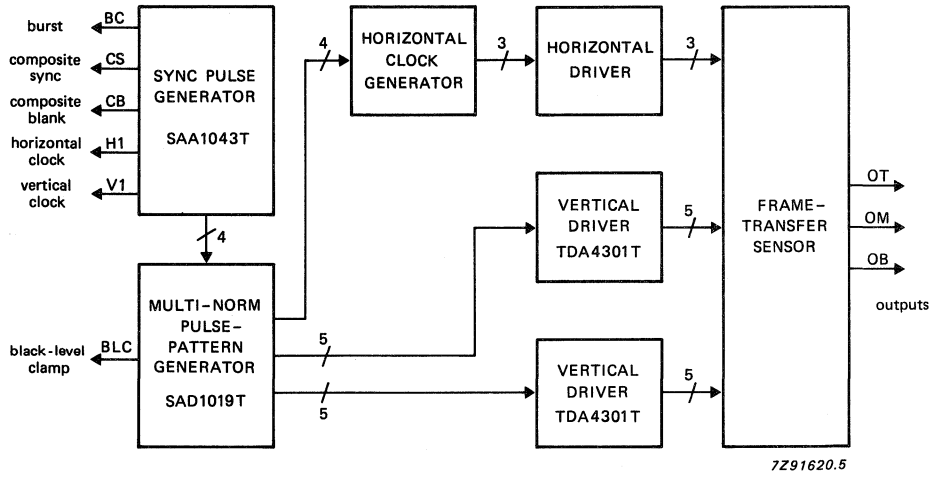


Fig. 17 Drive circuit for the NXA1011 frame transfer sensor.

FRAME TRANSFER SENSOR

GENERAL DESCRIPTION

The NXA1021 frame transfer sensor is a solid state imaging device which produces two interlaced 294-line fields (including 6 lines for dark reference and testing) with an aspect ratio of 4:3. The sensor is equipped with an on-chip colour stripe filter.
The device is compatible with PAL and SECAM TV standards and has a 7,5 mm image diagonal matching the half-inch camera tube format.

APPLICATIONS

- Consumer entertainment cameras
- Surveillance cameras – solid state reliability, high resolution and sensitivity provide the quality to be an ideal successor for your stripe filter camera tube
- Visual aids – the low voltage and mechanical ruggedness of this device allows design of safe and reliable cameras for visual aids
- Slide and film scanners for consumer applications

FEATURES

- Effective number of elements: 604 (horizontal) x 576 (vertical)
- Cyan, green, yellow and stripe filter on the chip
- Dark reference: 1 line per field for black clamping
- 100 x anti-blooming margin
- Gamma is 1
- High sensitivity, low noise
- Freedom from lag, burn-in, geometrical distortion and microphonic noise

DEVICE ORGANIZATION

- Frame transfer charge coupled device
- Unit cell size: 10 μm (horizontal) x 15,6 μm (vertical)
- Separate outputs for the cyan, green, and yellow channels
- Dummy elements: the first 5 elements of the 3 output registers are dummy elements
- On-chip high sensitivity output amplifier
- Image area: 6,0 mm (horizontal) x 4,5 mm (vertical)
- Chip size: 6,95 mm (horizontal) x 9,35 mm (vertical)

FUNCTIONAL DESCRIPTION

The special electrode arrangement allows 26% of the photosensitive element to be free of polysilicon. This facilitates easy penetration of the blue light into the element to provide good blue sensitivity.

The layout of the sensor is shown in Fig. 1.
It comprises 3 functional areas:

- a matrix of photosensitive elements and integration electrodes,
- a storage section,
- three BCCD read-out registers.

Figure 2 shows the transport process in the imaging and storage regions. At time t_0, the start of the first field read-out from the imaging region, $\phi 3$ is low and the charge is concentrated beneath $\phi 4$ to $\phi 2$. At t_1, $\phi 4$ goes low and the charge in each pixel concentrates beneath $\phi 1$ and $\phi 2$. At t_2, $\phi 3$ goes high and the charge packets advance one gate electrode, spreading out beneath $\phi 1$, $\phi 2$ and the following electrode $\phi 3$. In the next step, at t_3, $\phi 1$ goes low compressing the charge packets beneath $\phi 2$ and $\phi 3$, and at t_4, $\phi 4$ goes high allowing the charge packets again to advance one gate electrode. This process continues in both the imaging and storage regions until all the charge packets have transferred to the storage region.

The sensor in the integration mode is shown in Fig. 3. The first field is generated when phases $\phi 4$, $\phi 1$ and $\phi 2$ are high and $\phi 3$ is low, Fig. 3(a). $\phi 3$ effectively forms a potential barrier separating the pixels in the first field. The charges generated by incident light then integrate beneath $\phi 4$ and $\phi 2$, centred on $\phi 1$. So each pixel extends vertically over four gate electrodes.
The potential distribution of the second field, and hence its position relative to the first field is shown in Fig. 3(b). The second field is always displaced by two gate electrodes relative to the first field, with its charge patterns centred on $\phi 3$, and with $\phi 1$ forming the barrier between pixels, thus providing a perfectly interlaced frame structure.

CAUTION

The image sensor is a MOS device which can be destroyed by static charging of the gates. Always store the device with short-circuiting slamps or on conductive foam plastic. When cleaning the glass window only use alcohol or acetone. Rub the window carefully and slowly. Dry rubbing of the window may cause static charges which can destroy the device.

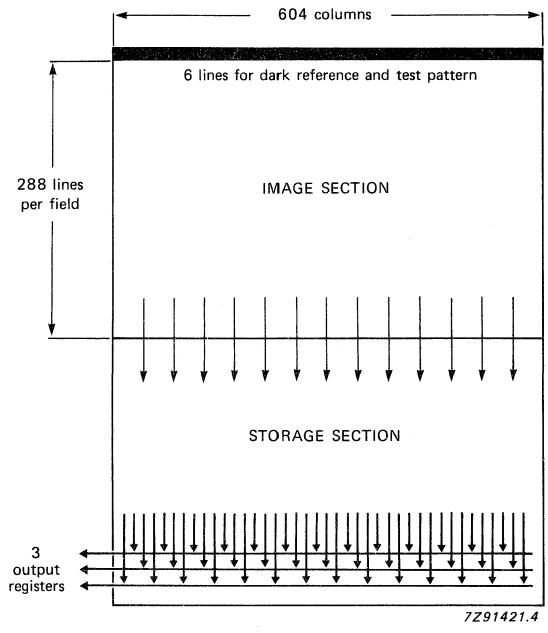


Fig. 1 Sensor layout and charge transport direction.

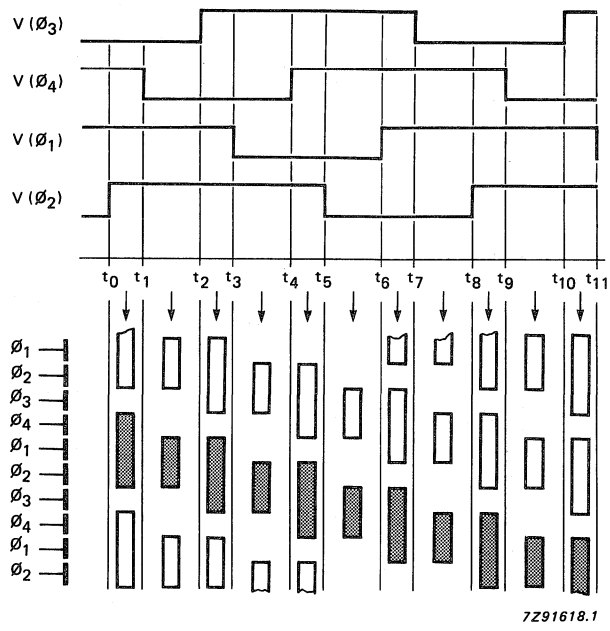


Fig. 2 Charge transport in the vertical direction.

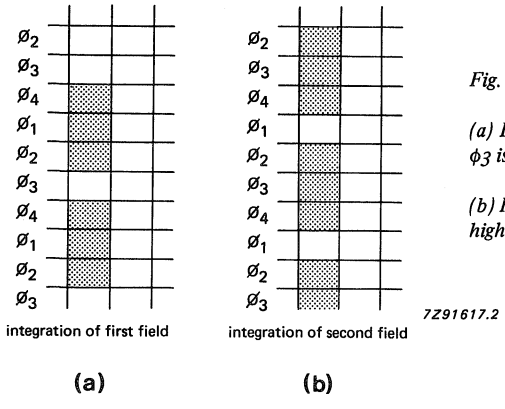


Fig. 3 Interlacing of the sensor.

(a) For integration of the first field, $\phi 4$ to $\phi 2$ are high, $\phi 3$ is low forming a barrier between charge packets.

(b) For integration of the second field, $\phi 2$ to $\phi 4$ are high, $\phi 1$ is low.

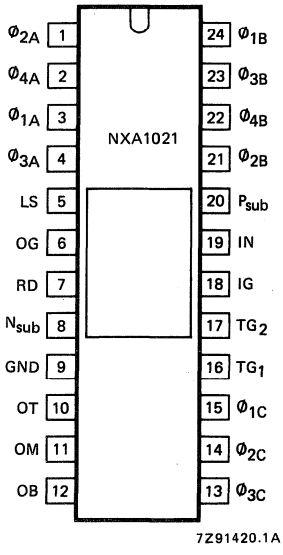


Fig. 4 Pin configuration.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	ϕ2A	Vertical transfer clocks for image part
2	ϕ4A	
3	ϕ1A	
4	ϕ3A	
5	LS	Light shield (Al. cover on storage part)
6	OG	Output gate
7	RD	Drain reset transistor
8	N_{sub}	N-substrate; supply voltage
9	GND	Ground
10	OT	Output top (cyan)
11	OM	Output middle (green)
12	OB	Output bottom (yellow)
13	ϕ3C	Horizontal transfer clock for output register
14	ϕ2C	
15	ϕ1C	
16	TG1	Transfer gate
17	TG2	
18	IG	Input gate (test point for manufacturing)
19	IN	Input diffusion (test point for manufacturing)
20	P_{sub}	P-substrate
21	ϕ2B	Vertical transfer clocks for storage part
22	ϕ4B	
23	ϕ3B	
24	ϕ1B	

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Voltages with respect to P_{sub}				
RD	$V_{RD-PSUB}$	−0,5	+25	V
IN	$V_{IN-PSUB}$	−0,5	+25	V
Voltages with respect to N_{sub}				
RD	$V_{RD-NSUB}$	−10	+0,5	V
IN	$V_{IN-NSUB}$	−10	+0,5	V
all other connections		−25	+0,5	V
Current from one output		−	10	mA
Storage temperature range	T_{stg}	−55	+80	°C
Operating ambient temperature range	T_{amb}	−40	+60	°C

DC CHARACTERISTICS at T_{amb} = 60 °C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Voltage at LS	V_{LS}	−	V_{Nsub}	−	V
Voltage at OG (note 1)	V_{OG}	4	−	7	V
Voltage at RD; current to sensor: $I < 1\ \mu A$	V_{RD}	15,5	16	16,5	V
Voltage at N_{sub}; $I < 10$ mA	V_{Nsub}	19,5	20	20,5	V
Voltage at IG	V_{IG}	−	GND	−	V
DC level of output voltage at OT, OM, OB (notes 2 and 3)	$V_{OT; OM; OB}$	6	−	15	V
Voltage at P_{sub}; (note 1) current from sensor: $I < 50\ \mu A$	V_{Psub}	2	−	5	V
Voltage at IN	V_{IN}	−	V_{Nsub}	−	V
Power dissipation	P	−	80	150	mW
Leakage current of gates	I_{I}	−	−	2.5	μA

Notes

1. These values must be adjusted to the optimum operating point within the given range.
2. Measured with output buffer. See Fig. 5.
3. See Fig. 16.

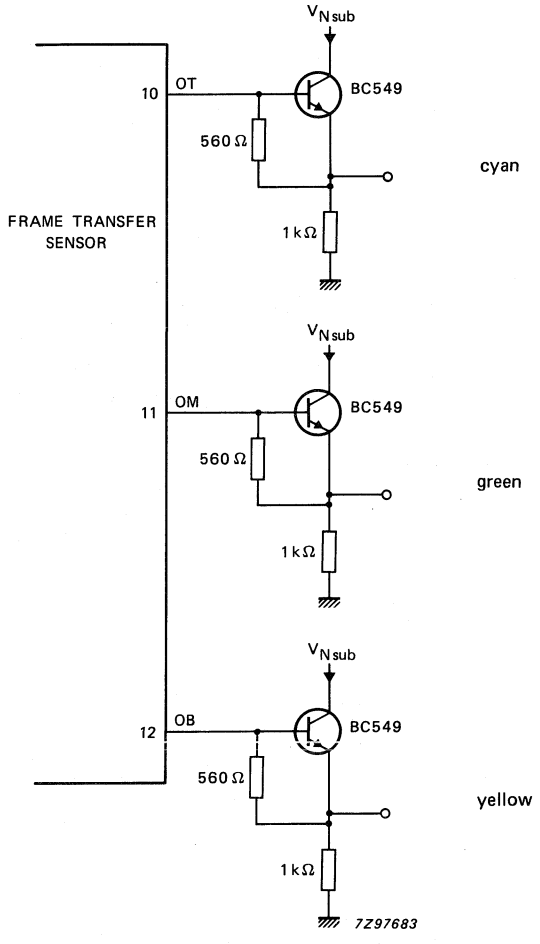


Fig. 5 Output buffer for measurements.

CLOCK CHARACTERISTICS (note 1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
LOW levels					
ϕnA, ϕnB	$V_{\phi nA/B}$	–	GND	–	–
ϕ_{1C}, ϕ_{2C}, ϕ_{3C} ($\phi_{1CLOW} = \phi_{2CLOW} = \phi_{3CLOW}$) (note 2)	$V_{\phi nC}$	0	3,5	5	V
TG1 (note 2)	V_{TG1}	0	1	4	V
TG2 (note 2)	V_{TG2}	0	6,5	8	V
Amplitudes					
ϕnA, ϕnB, ϕnC	$V_{\phi(p\text{-}p)}$	9,75	10	10,25	V
Timing (see Figs 6 and 7)					
Horizontal clocks					
clock frequency (note 3)	f_c	–	3,85	–	MHz
rise time	t_{rc}	20	–	40	ns
fall time	t_{fc}	20	–	40	ns
overlap time	t_{ihc}	10	–	–	ns
	t_{ilc}	5	–	–	ns
Vertical clocks					
clock frequency	f_{cv}	–	625	–	kHz
rise time	t_{rv}	–	50	–	ns
fall time	t_{fv}	–	70	–	ns
overlap time	t_{ihv}	80	100	120	ns
	t_{ilv}	100	200	260	ns
Transfer gates					
rise time	t_{rTG}	–	70	–	ns
fall time	t_{fTG}	–	100	–	ns
Clock capacitance					
Each clock phase ϕnA, ϕnB	$C_{\phi nA/B}$	–	–	3000	pF
ϕnC, TG1, TG2	$C_{\phi nC}$, $C_{TG1/2}$	–	–	100	pF
Leakage current of the clock connections	I_l	–	–	2,5	μA

Notes

1. Measured with output buffer. See Fig. 5.
2. These values must be adjusted to the optimum operating point within the given range.
3. Deviations from this frequency result in incorrect aspect ratio.

ADJUSTMENT OF OPERATING LEVELS

For optimum performance, fine adjustment of the sensors DC levels is essential. When carrying out this operation the following points should be considered.

- Vertical stripes in the picture are usually the result of charges being unevenly sorted into the three output registers. This can be influenced by offsets $V_{\phi C}$, V_{TG1}, V_{TG2} and V_{OG}.
- The anti-blooming performance of a sensor is influenced by its internal vertical potential gradient. This can be optimized by adjusting V_{Psub}.

DRIVING PULSE WAVEFORMS

The specifications of the sensor are measured when the following clock pulses are applied (Figs 6 and 7). In principle the sensor can be operated with different clock pulses, e.g. different clock frequencies (overlap conditions have to be maintained).

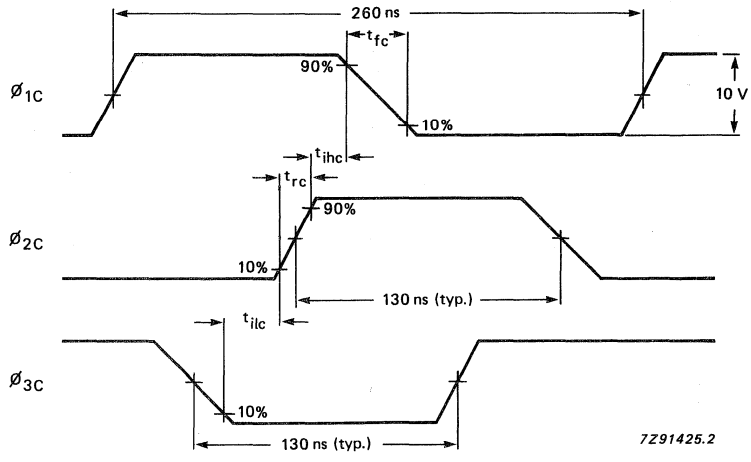


Fig. 6 Horizontal transport timing waveforms for the sensor electrodes (ϕ_{nC}); times measured at the 10% and 90% points of the amplitude.

DRIVING PULSE WAVEFORMS (continued)

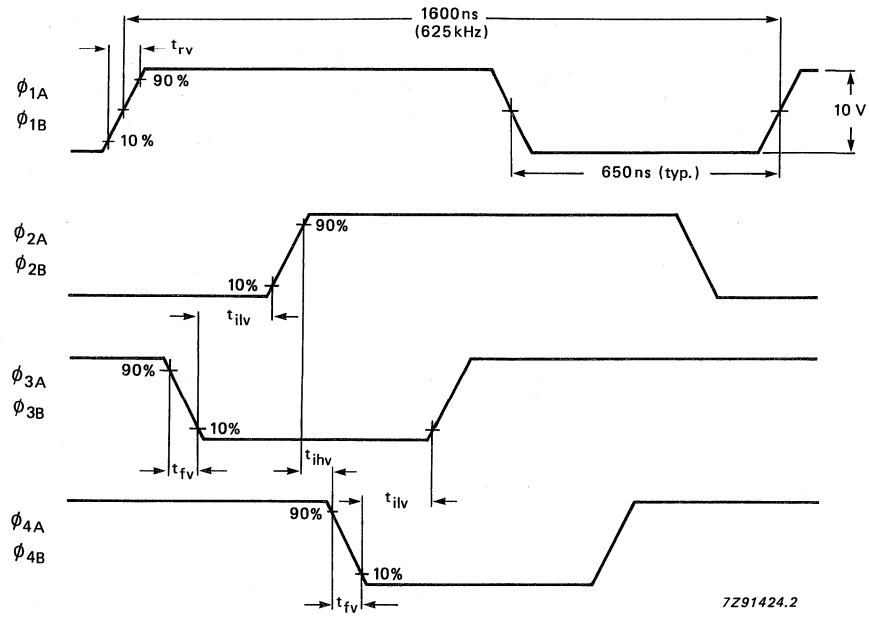


Fig. 7 Vertical transport timing waveforms for the sensor electrodes (ϕ_{nA}, ϕ_{nB}); times measured at the 10% and 90% points of the amplitude.

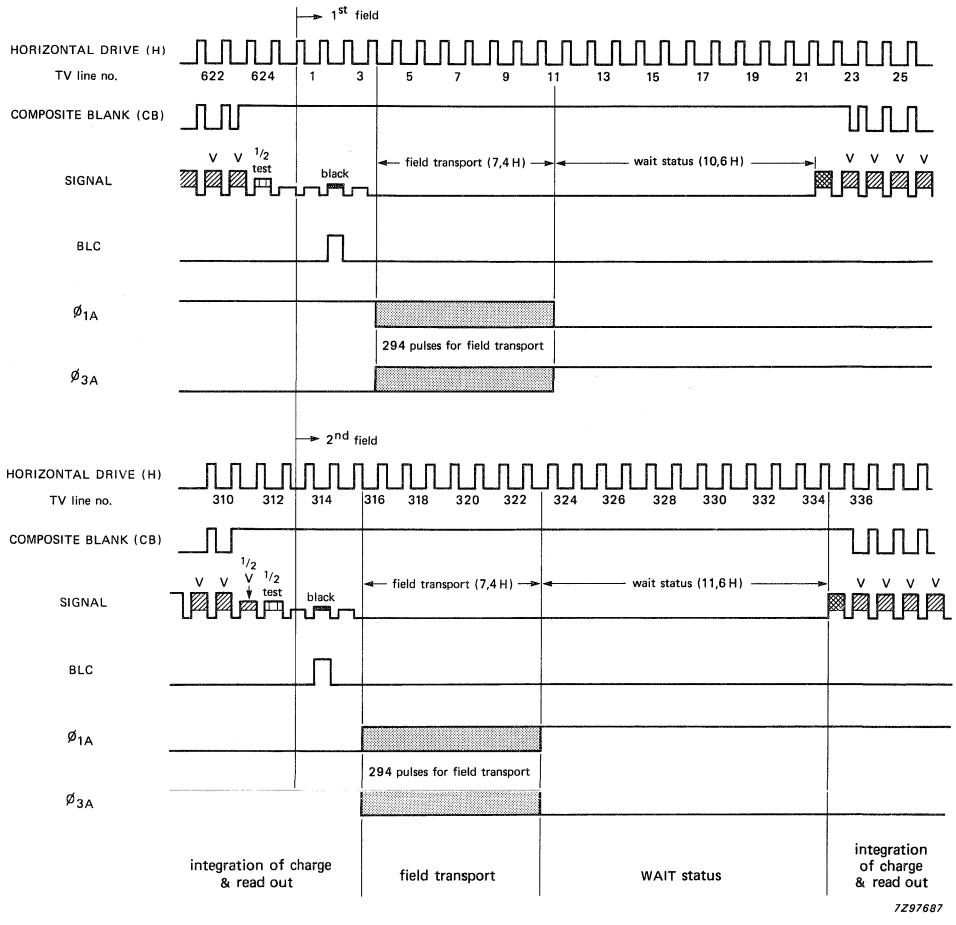


Fig. 8 Drive-pulse sequence and line numbering for field transport.

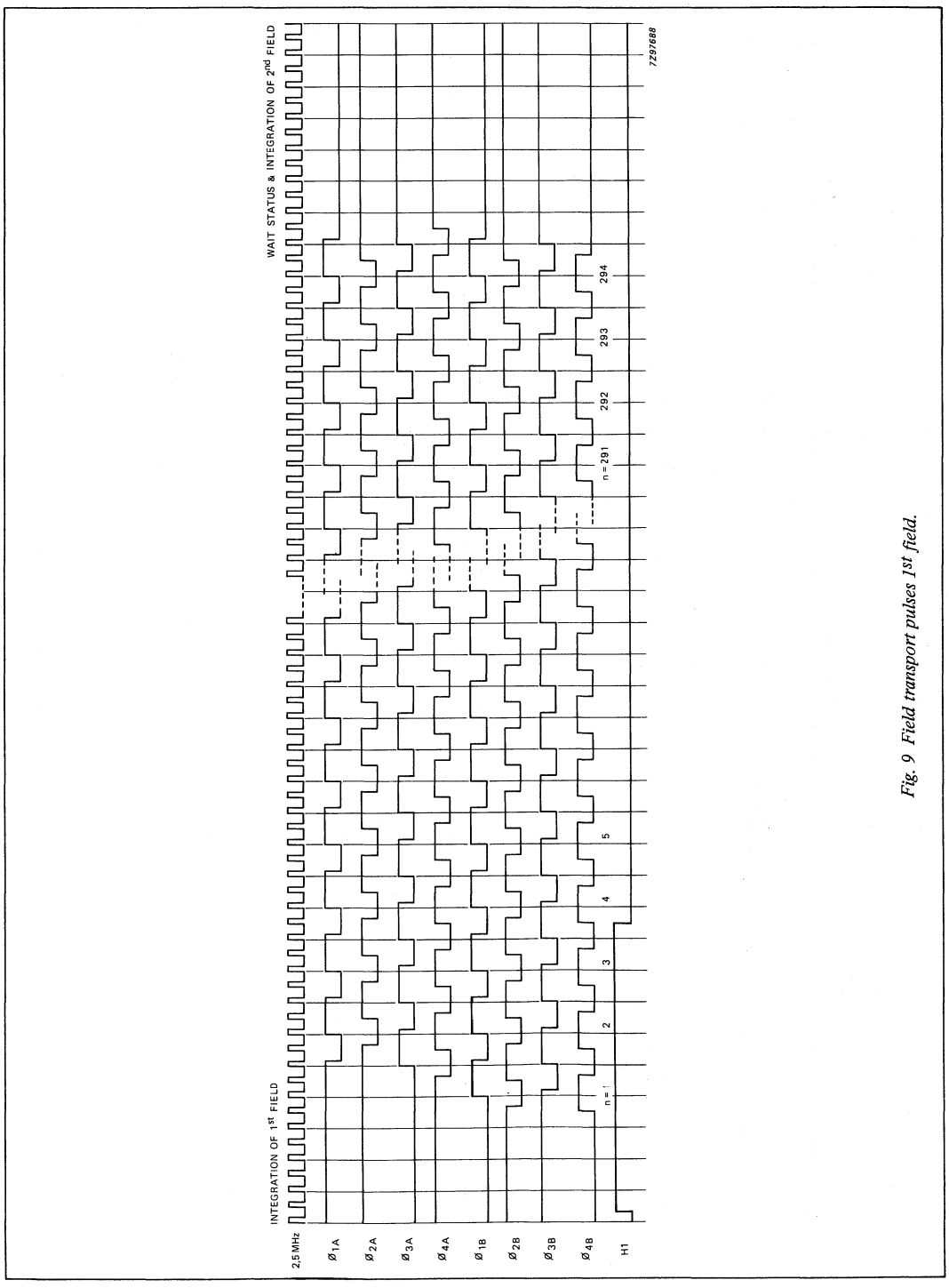


Fig. 9 Field transport pulses 1st field.

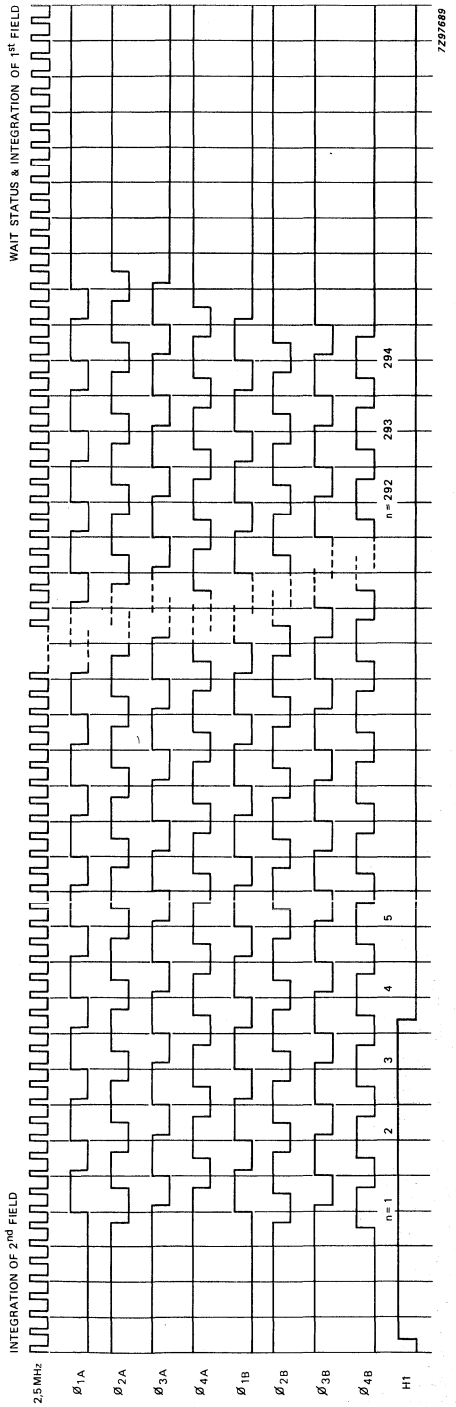


Fig. 10 Field transport pulses 2nd field.

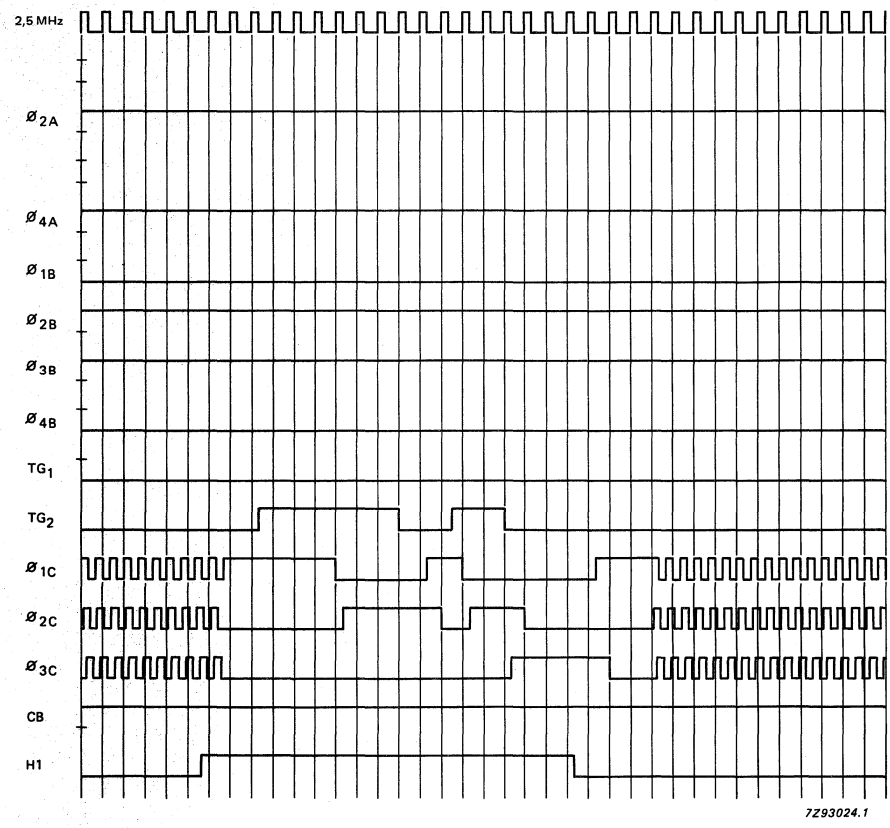


Fig. 11 Wait status.

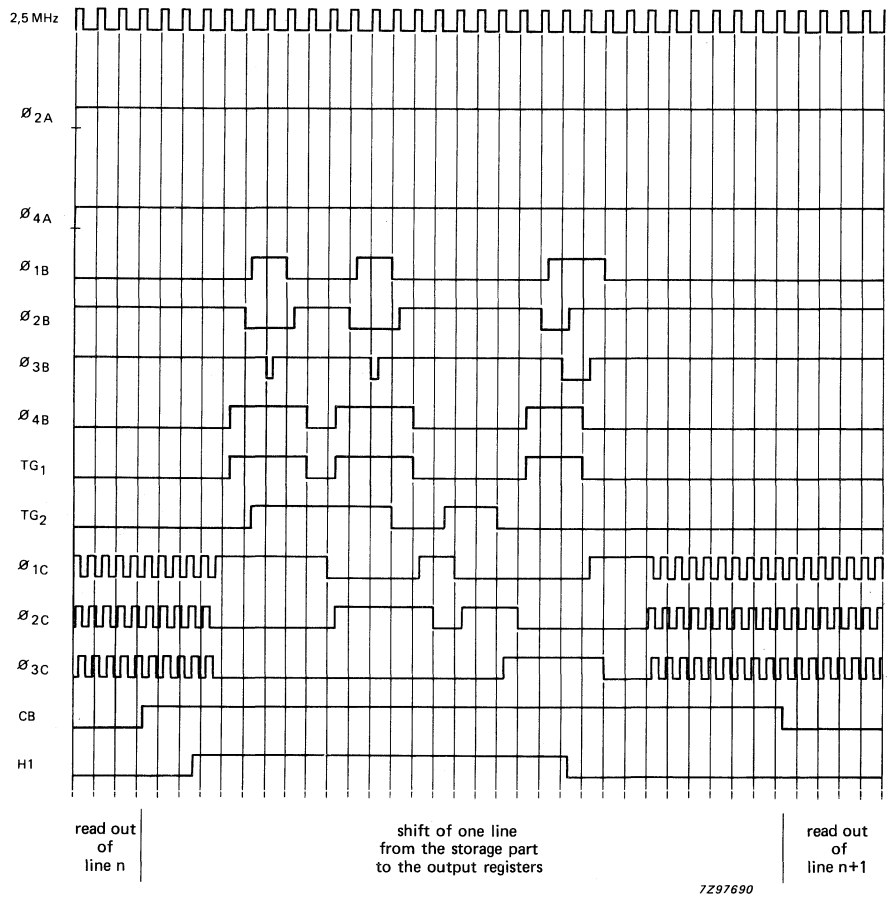


Fig. 12 Read-out of the output registers and sorting of the signal into output registers.

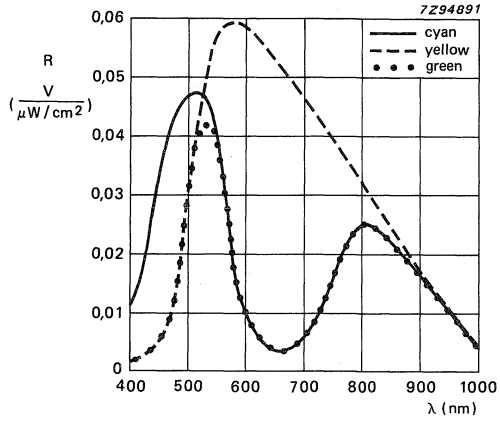


Fig. 13 Spectral response

OUTPUT CHARACTERISTICS at T_{amb} = 60 °C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Load capacitance	C_L	–	–	10	pF
Output signal voltage at standard illumination (peak-to-peak value) (see notes 1 and 2)					
Cyan channel	V_{OT}	30	–	–	mV
Green channel	V_{OM}	27	–	–	mV
Yellow channel	V_{OB}	60	–	–	mV
Output signal voltage at saturation (peak-to-peak value) (note 2)	V_{Osat}	300	600	1200	mV
Maximum illumination on the sensor without blooming (note 3)	E_B	2000	–	–	lx
Transport inefficiency					
horizontal one step	ϵ_H	–	–	$8{,}5 \times 10^{-5}$	
vertical one step	ϵ_V	–	–	5×10^{-5}	
Dark current	I_D	–	–	3	nA
Smear (note 4)					%

Notes

1. 5 lx on the sensor, colour temperature of light source 3200 K, Hoya-IR-Filter C500S, 1 mm is used.
2. Measured with output buffer.
3. See 'Defenition of blooming'.
4. See 'Defenition of smear'.

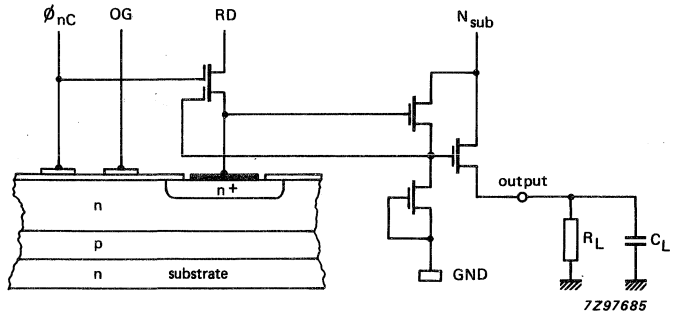


Fig. 14 Circuit diagram for one output channel.

DEFINITION OF SMEAR

During the field transport time the complete field is shifted over the image section. So each pixel of one column is illuminated by the light on all the other pixels of one column for a short time. Therefore a bright spot makes a bright vertical stripe on the image. This effect is called smear. The brightness of the stripe depends on the height of the spot and on the illumination of the spot.

It is defined by the equation:

$$V_{smear} = \frac{t_{field\ transport}}{t_{integration}} \times \frac{h}{H} \times \frac{E}{E_{sat}} \times V_{sat}$$

Where:

V_{smear} = Additional output voltage due to smear
$t_{field\ transport}$ = 0,47 ms
$t_{integration}$ = 19,5 ms
h = Height of bright spot
H = Height of the complete image
E = Illumination of the spot
E_{sat} = Saturation illumination
V_{sat} = Output voltage at saturation

Example:

Spot height is 10% of the height.
Spot illumination is 100% of saturation.

$$V_{smear} = \frac{0,47}{19,5} \times 0,1 \times 1 \times V_{sat} = 0,0024 \times V_{sat}$$

DEFINITION OF BLOOMING

When part of the image section (spot) is illuminated above saturation level and with the rest of the image dark, at a certain level of overexposure (2000 lx for the NXA1021), the area of the spot increases irregularly. This effect is called blooming.

PICTURE ELEMENT DEFECTS

picture quality at T_{amb} = 60 °C

GRADE	PIXEL DEFECTS (note 1)	CLUSTERS (note 2)	COLUMN DEFECTS (note 3)
01	0	0	0
02	2	0	0
03	10	2	0
04	35	5	2

Notes

1. A picture element is considered defect, if its signal deviates more than ±10% from the mean signal of the neighbouring picture element at standard illumination.
2. A cluster is a pair of two defect pixels at a distance of less than 3% of the picture height. The sum of pixel defects and clustered pixel defects does not exceed the number of permitted pixel defects. A pixel defect in the same place in odd and even fields is not defined as a cluster.
3. If more than two pixel defects occur in one column, this is considered a column defect.
   Additionally the indicated number of defect pixels is allowed.

OUTPUT SIGNAL

The output signal is a pulse sequence with a DC offset. The HIGH level of the output pulses, dependent upon the DC adjustments, varies between 6 and 15 volts. The LOW levels depend upon the signal voltage, itself a function of the intensity of the light falling on the sensor, and is between 1.0 and 0.2 volts below the HIGH level. These pulses contain the video information and need further processing to be converted into a signal suitable for use in standard video circuitry.

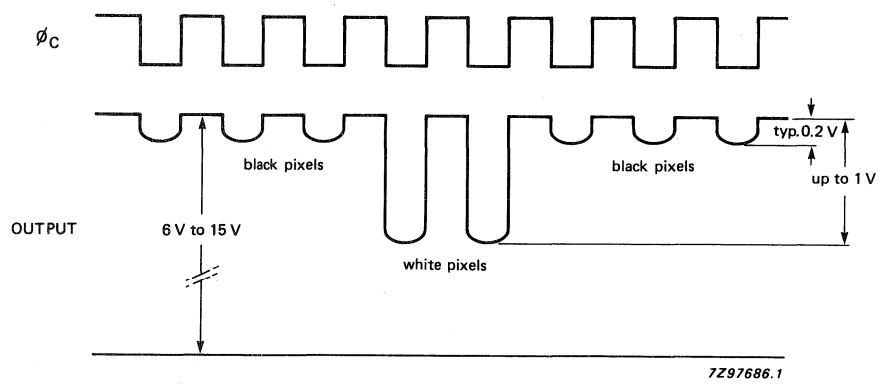


Fig. 15 Typical signal at the sensor output.

MECHANICAL PARAMETERS

The sensor is encapsulated in a 24-lead dual in-line ceramic package with a high-quality glass viewing window on the top side for admittance of light to the sensor.

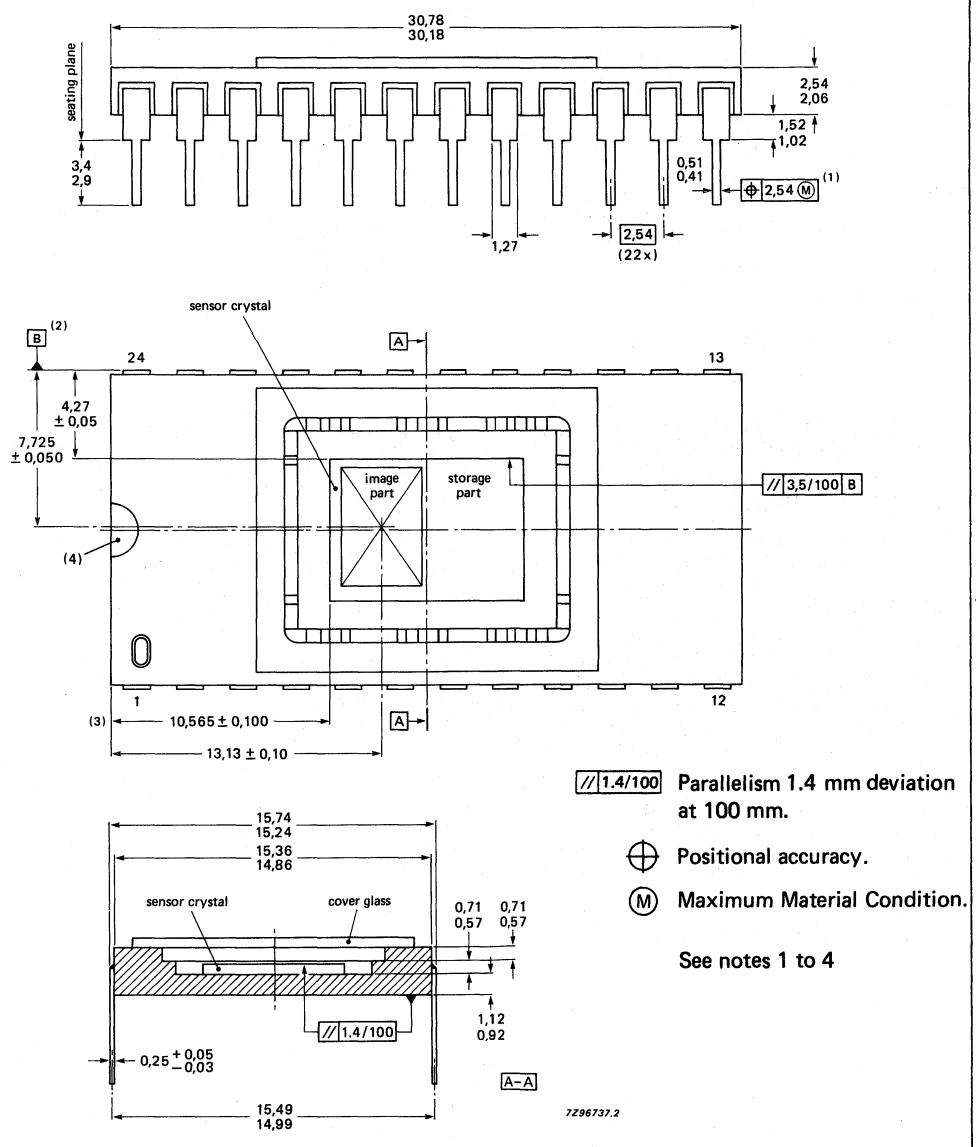


Fig. 16 Package outline; dimensions in mm (also see notes).

Notes to Fig. 16

1. Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.
2. Line B is the connection line between pins 13 and 24. Pins 14 to 23 are not necessarily exactly on this line.
3. These two dimensions are measured at the centre-line of the package.
4. The gold plateau is internally connected to N_{sub}.

GENERAL DIMENSIONS (See Fig. 16)

Chip thickness	525 ± 15 μm
Cover glass thickness	550 ± 50 μm
Thickness of glue layer between sensor and cavity bottom	80 ± 30 μm
Refractive index	1,5
Transmission (400-700 nm)	90%

Sensor is filled with nitrogen.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or Wave

The maximum permissable temperature of the solder is 260 °C, this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the seating plane but the temperature of the ceramic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

APPLICATION INFORMATION

Figure 17 shows a circuit for providing the pulse sequences needed to drive the sensor. A SAA1043 sync-pulse generator provides the three TV standards, namely PAL, SECAM and NTSC. These include vertical and horizontal blanking, and black-level clamping. It also provides other signals essential for tv camera operation and can be triggered externally for operation with, for example, a VCR or computer. The sync-pulse generator drives a SAD1019 multi-norm pulse-pattern generator (MNPPG) developed specifically for the image sensors. It provides all the clock signals except the pulses for the horizontal read-out registers. Its use avoids the need to develop complex circuitry for driving the NXA1021. Fast clock pulses for the three horizontal read-out registers are generated by a horizontal clock generator. The three 3.85 MHz pulse trains generated differ in phase by 120°. The output levels from the MNPPG are too low to drive the shift registers directly, therefore, additional vertical driver IC's (VDR) TDA4301 are required to boost these signals to suitable levels. During the horizontal blanking period, slow pulses derived from the MNPPG need to be applied to the horizontal registers to sort the charge packets into the three horizontal read out registers.

More detailed information is available on request.

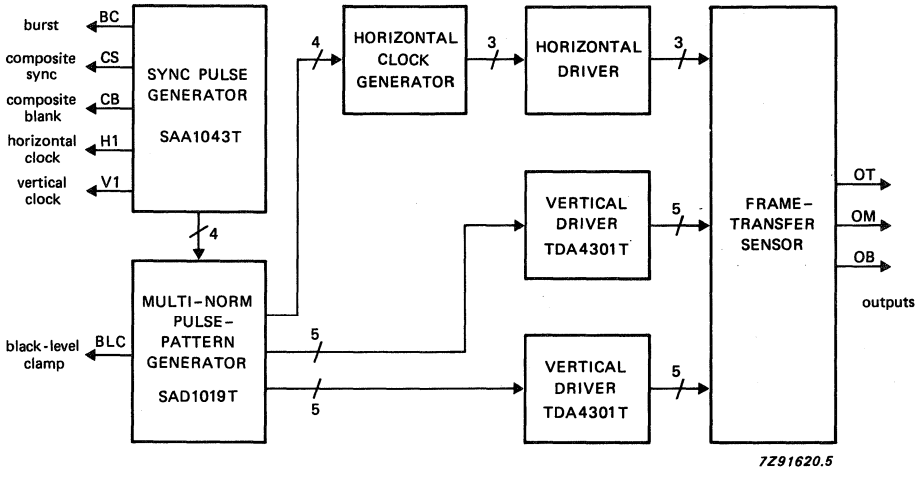


Fig. 17 Drive circuit for the NXA1021 frame transfer sensor.

FRAME TRANSFER SENSOR

GENERAL DESCRIPTION

The NXA1031 frame transfer sensor is a solid state imaging device which produces two interlaced 251-line fields (including 6 lines for dark reference and testing) with an aspect ratio of 4:3.
The device is compatible with EIA TV standards and has a 7,5 mm image diagonal matching the half-inch camera tube format. The NXA1031 can be supplied without glass window upon consultation.

APPLICATIONS

- ENG cameras – the high blue sensitivity and good horizontal resolution makes this sensor suiteable for 3-chip ENG colour cameras
- Surveillance cameras – solid state reliability, high resolution and sensitivity provide the quality to be an ideal successor for the Newvicon® or Ultricon® pick-up element
- Character and pattern recognition – the excellent linearity and uniformity recommends this sensor as a first choice for these applications
- Robotics – the small size, light-weight and mechanical ruggedness makes this sensor extremely suitable for all types of high resolution robot-vision applications
- Visual aids – the low voltage and mechanical ruggedness of this device allows design of safe and reliable cameras for visual aids

FEATURES

- Effective number of elements: 610 (horizontal) x 490 (vertical)
- Dark reference: 1 line per field for black clamping
- 100 x anti-blooming margin
- Gamma is 1
- High sensitivity, low noise
- Freedom from lag, burn-in, geometrical distortion and microphonic noise

DEVICE ORGANIZATION

- Frame transfer charge coupled device
- Unit cell size: 9,9 μm (horizontal) x 18,6 μm (vertical)
- Dummy elements: the first 5 elements of the 3 output registers are dummy elements
- On-chip high sensitivity output amplifier
- Image area: 6,0 mm (horizontal) x 4,5 mm (vertical)
- Chip size: 6,95 mm (horizontal) x 9,35 mm (vertical)

FUNCTIONAL DESCRIPTION

The special electrode arrangement allows 35% of the photosensitive element to be free of polysilicon. This facilitates easy penetration of the blue light into the element to provide good blue sensitivity.

The layout of the sensor is shown in Fig. 1.
It comprises 3 functional areas:

- a matrix of photosensitive space elements and integration electrodes,
- a storage section,
- three BCCD read-out registers.

Figure 2 shows the transport process in the imaging and storage regions. At time t_0, the start of the first field read-out from the imaging region, ϕ_3 is low and the charge is concentrated beneath ϕ_4 to ϕ_2. At t_1, ϕ_4 goes low and the charge in each pixel concentrates beneath ϕ_1 and ϕ_2. At t_2, ϕ_3 goes high and the charge packets advance one gate electrode, spreading out beneath ϕ_1, ϕ_2 and the following electrode ϕ_3. In the next step, at t_3, ϕ_1 goes low compressing the charge packets beneath ϕ_2 and ϕ_3, and at t_4, ϕ_4 goes high allowing the charge packets again to advance one gate electrode. This process continues in both the imaging and storage regions until all the charge packets have transferred to the storage region.

The sensor in the integration mode is shown in Fig. 3. The first field is generated when phases ϕ_4, ϕ_1 and ϕ_2 are high and ϕ_3 is low, Fig. 3(a). ϕ_3 effectively forms a potential barrier separating the pixels in the first field. The charges generated by incident light then integrate beneath ϕ_4 and ϕ_2, centred on ϕ_1. So each pixel extends vertically over four gate electrodes.
The potential distribution of the second field, and hence its position relative to the first field is shown in Fig. 3(b). The second field is always displaced by two gate electrodes relative to the first field, with its charge patterns centred on ϕ_3, and with ϕ_1 forming the barrier between pixels, thus providing a perfectly interlaced frame structure.

CAUTION

The image sensor is a MOS device which can be destroyed by static charging of the gates. Always store the device with short-circuiting clamps or on conductive foam plastic. When cleaning the glass window only use alcohol or acetone. Rub the window carefully and slowly. Dry rubbing of the window may cause static charges which can destroy the device.

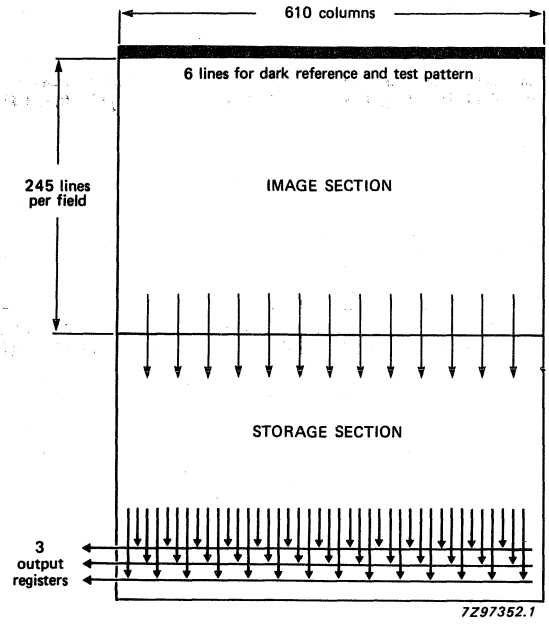


Fig. 1 Sensor layout and charge transport direction.

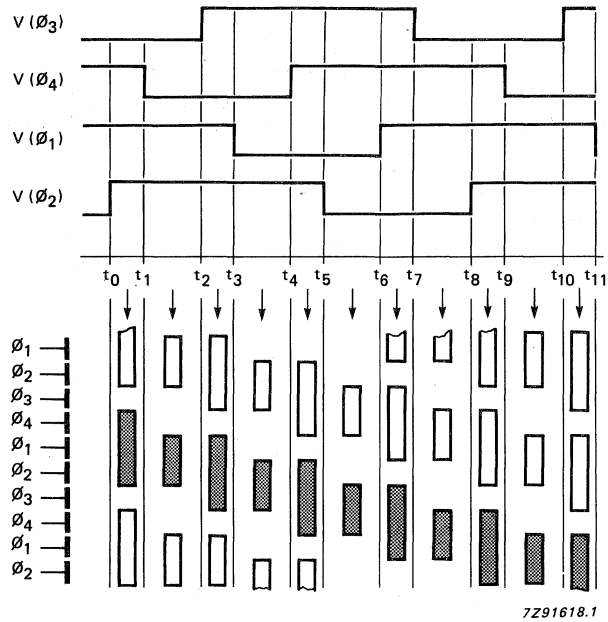


Fig. 2 Charge transport in the vertical direction.

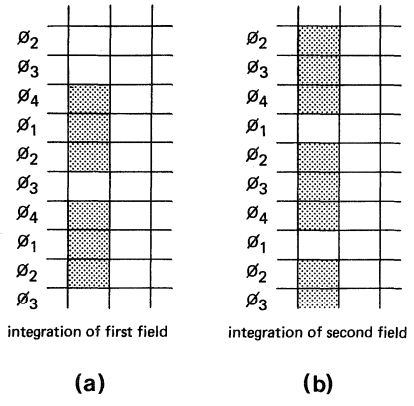


Fig. 3 Interlacing of the sensor.

(a) For integration of the first field, ϕ_4 to ϕ_2 are high, ϕ_3 is low forming a barrier between charge packets.

(b) For integration of the second field, ϕ_2 to ϕ_4 are high, ϕ_1 is low.

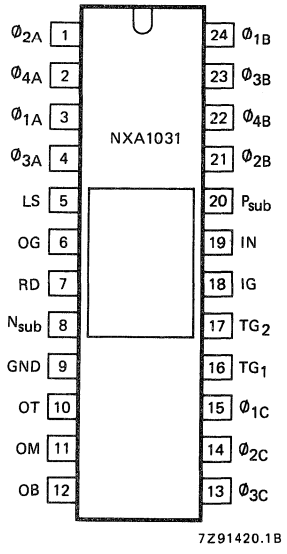


Fig. 4 Pin configuration.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	ϕ_{2A}	Vertical transfer clocks for image part
2	ϕ_{4A}	
3	ϕ_{1A}	
4	ϕ_{3A}	
5	LS	Light shield (A1, cover on storage part)
6	OG	Output gate
7	RD	Drain reset transistor
8	N_{sub}	N-substrate; supply voltage
9	GND	Ground
10	OT	Output top
11	OM	Output middle
12	OB	Output bottom
13	ϕ_{3C}	Horizontal transfer clock for output register
14	ϕ_{2C}	
15	ϕ_{1C}	
16	TG1	Transfer gates
17	TG2	
18	IG	Input gate (test point for manufacturing)
19	IN	Input diffusion (test point for manufacturing)
20	P_{sub}	P-substrate
21	ϕ_{2B}	Vertical transfer clocks for storage part
22	ϕ_{4B}	
23	ϕ_{3B}	
24	ϕ_{1B}	

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Voltages with respect to P_{sub}				
RD	$V_{RD-PSUB}$	−0,5	+25	V
IN	$V_{IN-PSUB}$	−0,5	+25	V
Voltages with respect to N_{sub}				
RD	$V_{RD-NSUB}$	−10	+0,5	V
IN	$V_{IN-NSUB}$	−10	+0,5	V
all other connections		−25	+0,5	V
Current from one output		−	10	mA
Storage temperature range	T_{stg}	−55	+80	°C
Operating ambient temperature range	T_{amb}	−40	+60	°C

DC CHARACTERISTICS at T_{amb} = 60 °C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Voltage at LS	V_{LS}	−	V_{Nsub}	−	V
Voltage at OG (note 1)	V_{OG}	4	−	7	V
Voltage at RD; current to sensor: $I < 1\ \mu A$	V_{RD}	15,5	16	16,5	V
Voltage at N_{sub}; $I < 10$ mA	V_{Nsub}	19,5	20	20,5	V
Voltage at IG	V_{IG}	−	GND	−	V
DC level of output voltage at OT, OM, OB (notes 2 and 3)	$V_{OT; OM; OB}$	6	−	15	V
Voltage at P_{sub}; (note 1) current from sensor: $I < 50\ \mu A$	V_{Psub}	2	−	5	V
Voltage at IN	V_{IN}	−	V_{Nsub}	−	V
Power dissipation	P	−	80	150	mW
Leakage current of gates	I_I	−	−	2.5	μA

Notes

1. These values must be adjusted to the optimum operating point within the given range.
2. Measured with output buffer. See Fig. 5.
3. See Fig. 16.

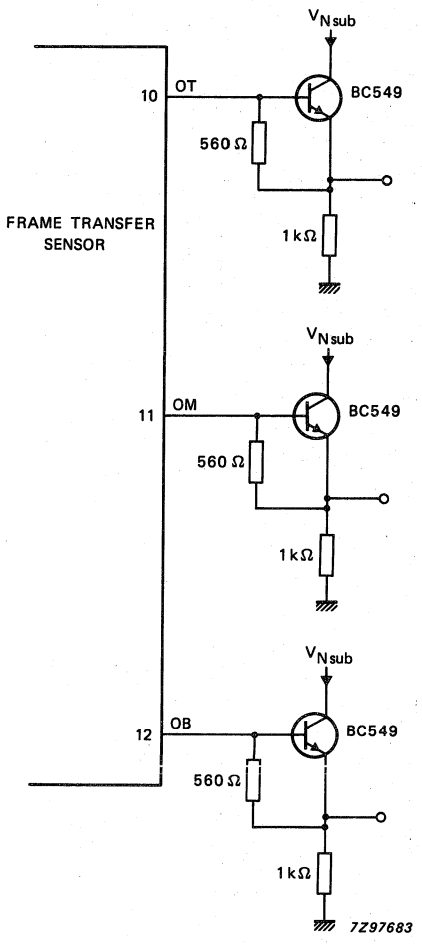


Fig. 5 Output buffer for measurements.

CLOCK CHARACTERISTICS (note 1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
LOW levels					
ϕnA, ϕnB	$V_{\phi nA/B}$	–	GND	–	–
ϕ_{1C}, ϕ_{2C}, ϕ_{3C} ($\phi_{1CLOW} = \phi_{2CLOW} = \phi_{3CLOW}$) (note 2)	$V_{\phi nC}$	0	3,5	5	V
TG1 (note 2)	V_{TG1}	0	1	4	V
TG2 (note 2)	V_{TG2}	0	6,5	8	V
Amplitudes					
ϕnA, ϕnB, ϕnC	$V_{\phi(p\text{-}p)}$	9,75	10	10,25	V
Timing (see Figs 6 and 7)					
Horizontal clocks					
clock frequency (note 3)	f_c	–	3,90	–	MHz
rise time	t_{rc}	20	–	40	ns
fall time	t_{fc}	20	–	40	ns
overlap time	t_{ihc}	10	–	–	ns
	t_{ilc}	5	–	–	ns
Vertical clocks					
clock frequency	f_{cv}	–	629	–	kHz
rise time	t_{rv}	–	50	–	ns
fall time	t_{fv}	–	70	–	ns
overlap time	t_{ihv}	80	100	120	ns
	t_{ilv}	100	200	260	ns
Transfer gates					
rise time	t_{rTG}	–	70	–	ns
fall time	t_{fTG}	–	100	–	ns
Clock capacitance					
Each clock phase ϕnA, ϕnB	$C_{\phi nA/B}$	–	–	3000	pF
ϕnC, TG1, TG2	$C_{\phi nC}$, $C_{TG1/2}$	–	–	100	pF
Leakage current of the clock connections	I_l	–	–	2,5	μA

Notes

1. Measured with output buffer. See Fig. 5.
2. These values must be adjusted to the optimum operating point within the given range.
3. Deviations from this frequency result in incorrect aspect ratio.

ADJUSTMENT OF OPERATING LEVELS

For optimum performance, fine adjustment of the sensors DC levels is essential. When carrying out this operation the following points should be considered.

- Vertical stripes in the picture are usually the result of charges being unevenly sorted into the three output registers. This can be influenced by offsets $V_{\phi C}$, V_{TG1}, V_{TG2} and V_{OG}.
- The anti-blooming performance of a sensor is influenced by its internal vertical potential gradient. This can be optimized by adjusting V_{Psub}.

DRIVING PULSE WAVEFORMS

The specifications of the sensor are measured when the following clock pulses are applied (Figs 6 and 7). In principle the sensor can be operated with different clock pulses, e.g. different clock frequencies (overlap conditions have to be maintained).

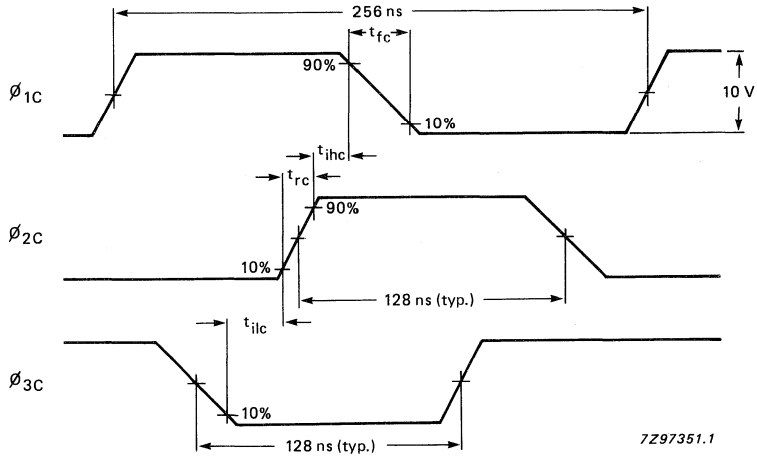


Fig. 6 Horizontal transport timing waveforms for the sensor electrodes (ϕ_{nC}); times measured at the 10% and 90% points of the amplitude.

DRIVING PULSE WAVEFORMS (continued)

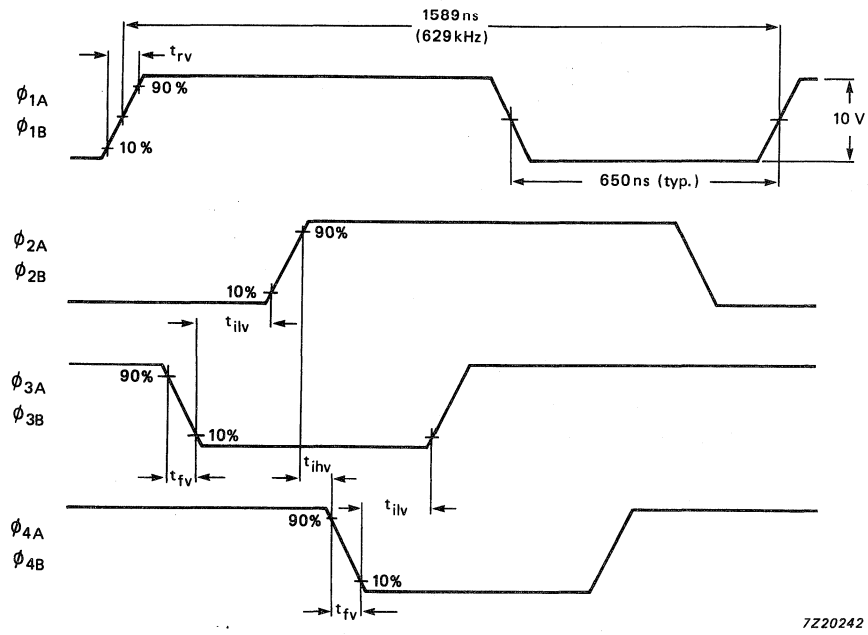


Fig. 7 Vertical transport timing waveforms for the sensor electrodes (ϕ_{nA}, ϕ_{nB}); times measured at the 10% and 90% points of the amplitude.

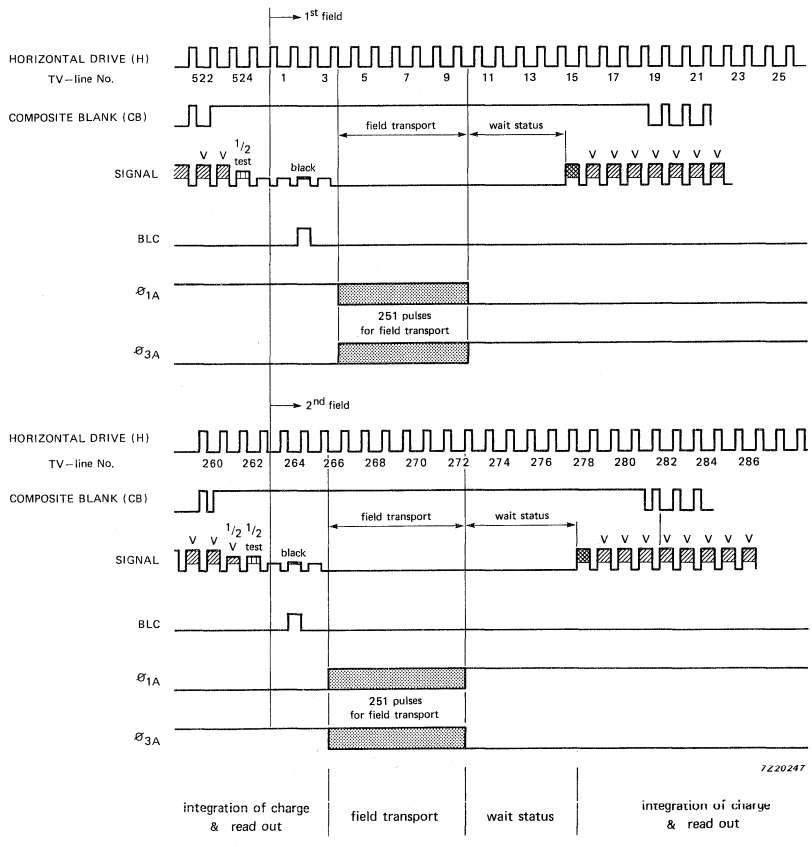


Fig. 8 Drive-pulse sequence and line numbering for field transport.

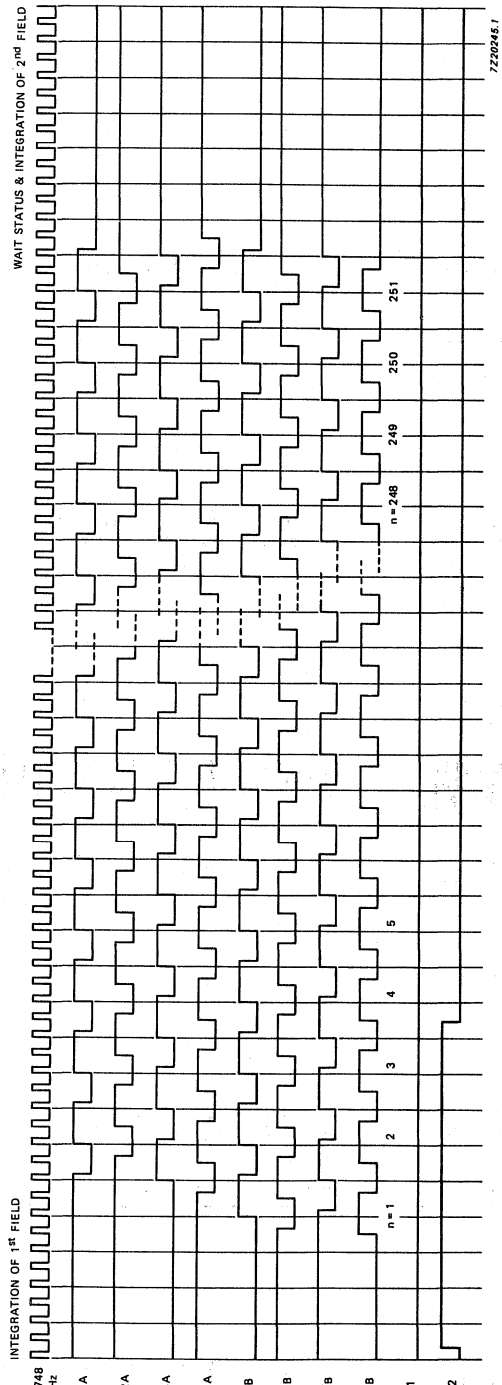


Fig. 9 Field transport pulses 1st field.

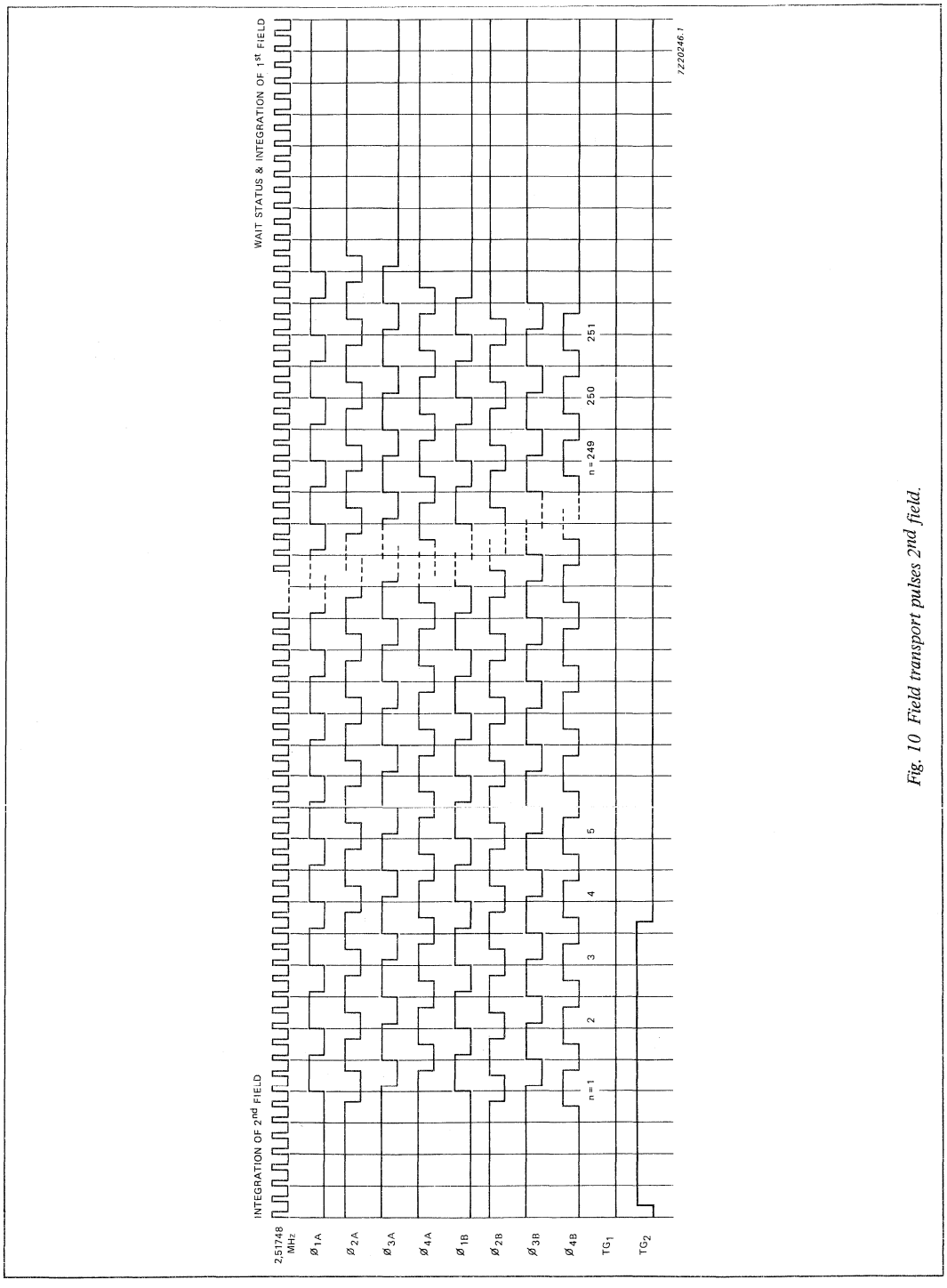


Fig. 10 Field transport pulses 2nd field.

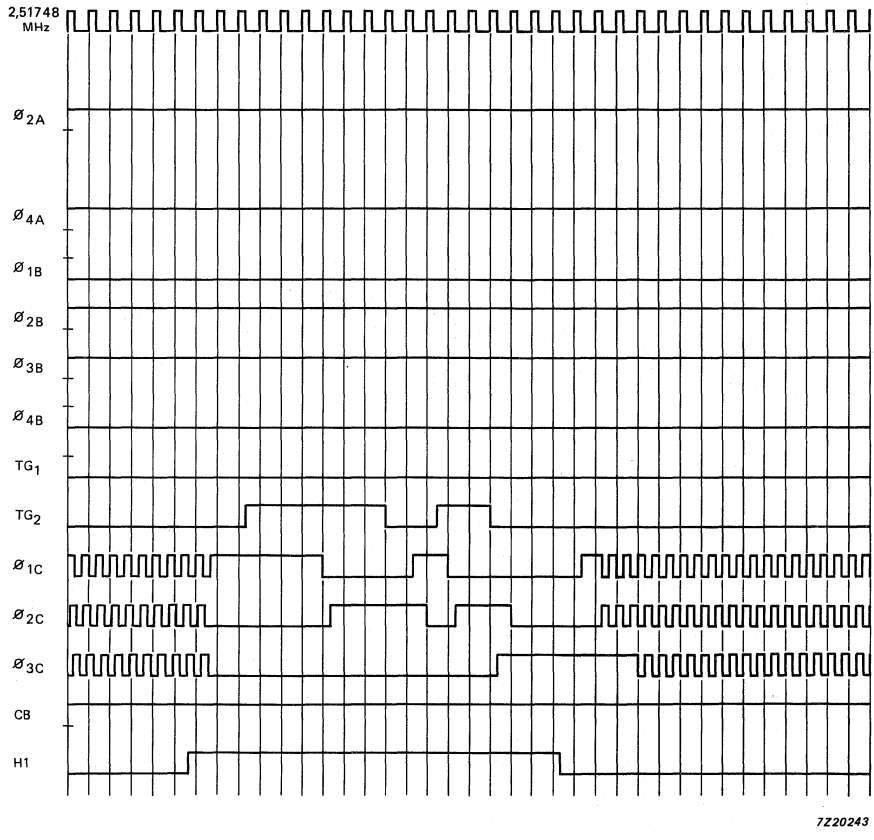


Fig. 11 Wait status.

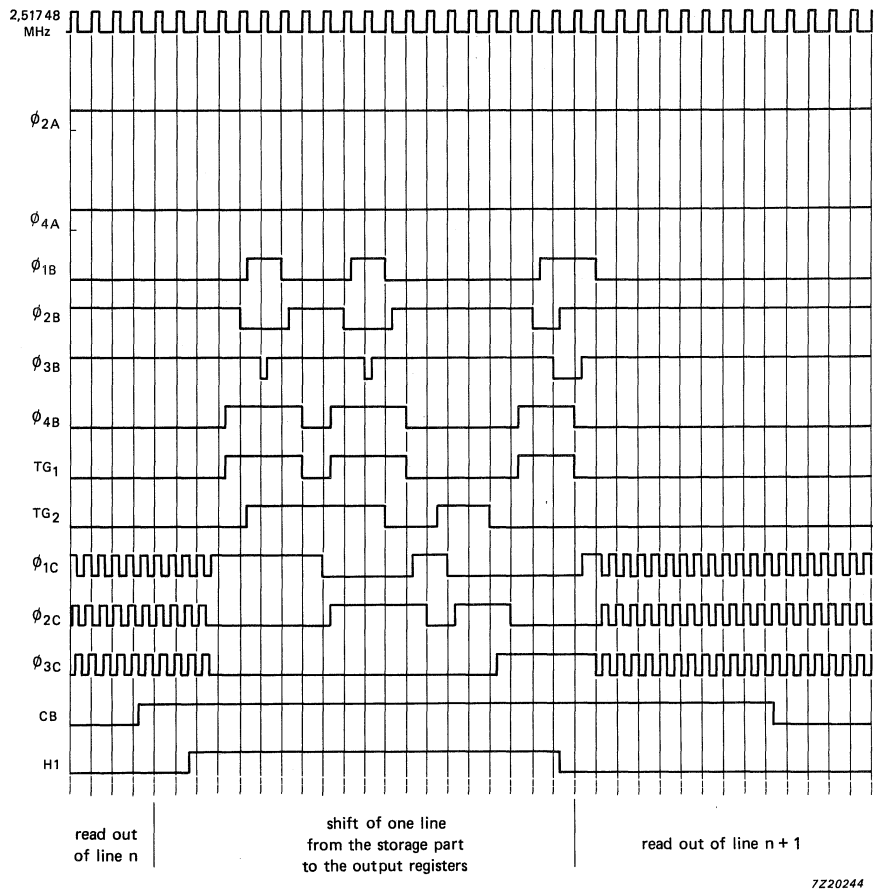


Fig. 12 Read out of the output registers and sorting of the signal into output registers.

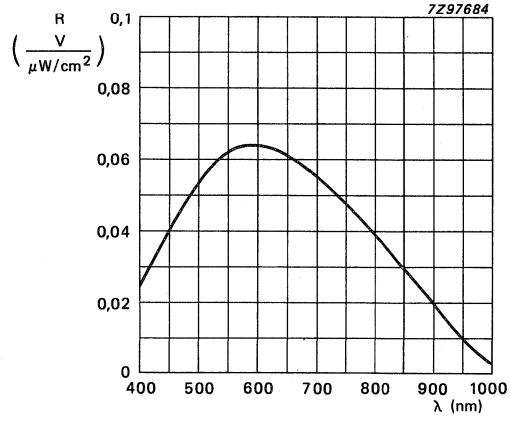


Fig. 13 Spectral response.

OUTPUT CHARACTERISTICS at T_{amb} = 60 °C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Load capacitance	C_L	–	–	10	pF
Output signal voltage at standard illumination (peak-to-peak value) (S/N typ. 50 dB) (notes 1 and 2)	V_{OTS} V_{OMS} V_{OBS}	70	100	–	mV
Signal to noise ratio at standard illumination (notes 1, 2 and 3)	S/N	–	50	–	dB
Output signal voltage at saturation (peak-to-peak value) (note 2)	V_{Osat}	300	600	1200	mV
Maximum illumination on the sensor without blooming (note 4)	E_B	2000	–	–	lx
Transport inefficiency horizontal one step vertical one step	 ϵ_H ϵ_V	 – –	 – –	 $8{,}5 \times 10^{-5}$ 5×10^{-5}	
Dark current	I_D	–	–	3	nA
Smear (note 5)					%

Notes

1. 5 Lx on the sensor, colour temperature of light source 3200 K, Hoya-IR-filter C500S, 1 mm is used.
2. Measured with output buffer.
3. 200 kHz to 5 MHz, weighted, T_{amb} = 25 °C
4. See 'Definition of blooming'.
5. See 'Definition of smear'.

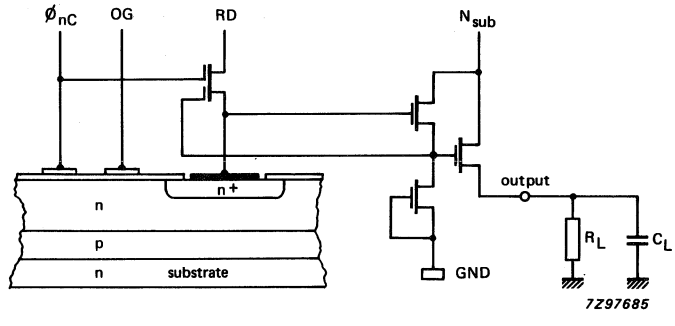


Fig. 14 Circuit diagram for one output channel.

DEFINITION OF SMEAR

During the field transport time the complete field is shifted over the image section. So each pixel of one column is illuminated by the light on all the other pixels of one column for a short time. Therefore a bright spot makes a bright vertical stripe on the image. This effect is called smear. The brightness of the stripe depends on the height of the spot and on the illumination of the spot.

It is defined by the equation:

$$V_{smear} = \frac{t_{field\ transport}}{t_{integration}} \times \frac{h}{H} \times \frac{E}{E_{sat}} \times V_{sat}$$

Where:

V_{smear}	= Additional output voltage due to smear
$t_{field\ transport}$	= 0,4 ms
$t_{integration}$	= 16,2 ms
h	= Height of bright spot
H	= Height of the complete image
E	= Illumination of the spot
E_{sat}	= Saturation illumination
V_{sat}	= Output voltage at saturation

Example:

Spot height is 10% of the height.
Spot illumination is 100% of saturation.

$$V_{smear} = \frac{0,4}{16,2} \times 0,1 \times 1 \times V_{sat} = 0,0024 \times V_{sat}$$

DEFINITION OF BLOOMING

When part of the image section (spot) is illuminated above saturation level and with the rest of the image dark, at a certain level of overexposure (2000 lx for the NXA1031), the area of the spot increases irregularly. This effect is called blooming.

PICTURE ELEMENT DEFECTS

picture quality at T_{amb} = 60 °C

GRADE	PIXEL DEFECTS (note 1)	CLUSTERS (note 2)	COLUMN DEFECTS (note 3)
01	0	0	0
02	2	0	0
03	10	2	0
04	35	5	2

Notes

1. A picture element is considered defect, if its signal deviates more than ±10% from the mean signal of the neighbouring picture element at standard illumination.
2. A cluster is a pair of two defect pixels at a distance of less than 3% of the picture height. The sum of pixel defects and clustered pixel defects does not exceed the number of permitted pixel defects. A pixel defect in the same place in odd and even fields is not defined as a cluster.
3. If more than two pixel defects occur in one column, this is considered a column defect.
   Additionally the indicated number of defect pixels is allowed.

OUTPUT SIGNAL

The output signal is a pulse sequence with a DC offset. The HIGH level of the output pulses, dependent upon the DC adjustments, varies between 6 and 15 volts. The LOW levels depend upon the signal voltage, itself a function of the intensity of the light falling on the sensor, and is between 1.0 and 0.2 volts below the HIGH level. These pulses contain the video information and need further processing to be converted into a signal suitable for use in standard video circuitry.

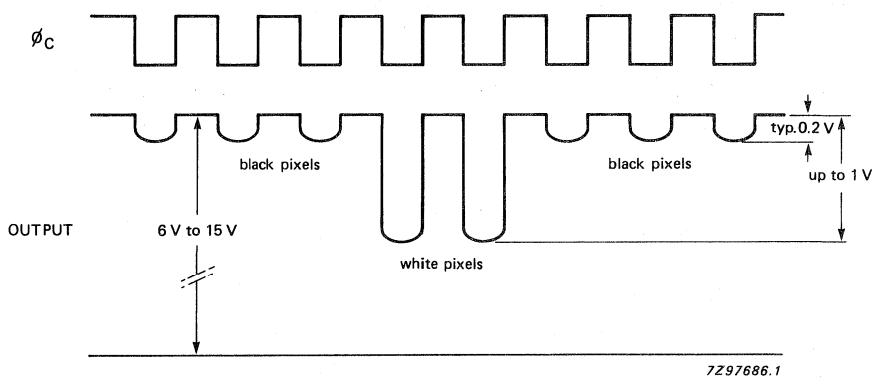


Fig. 15 Typical signal at the sensor output.

MECHANICAL PARAMETERS

The sensor is encapsulated in a 24-lead dual in-line ceramic package with a high-quality glass viewing window on the top side for admittance of light to the sensor.

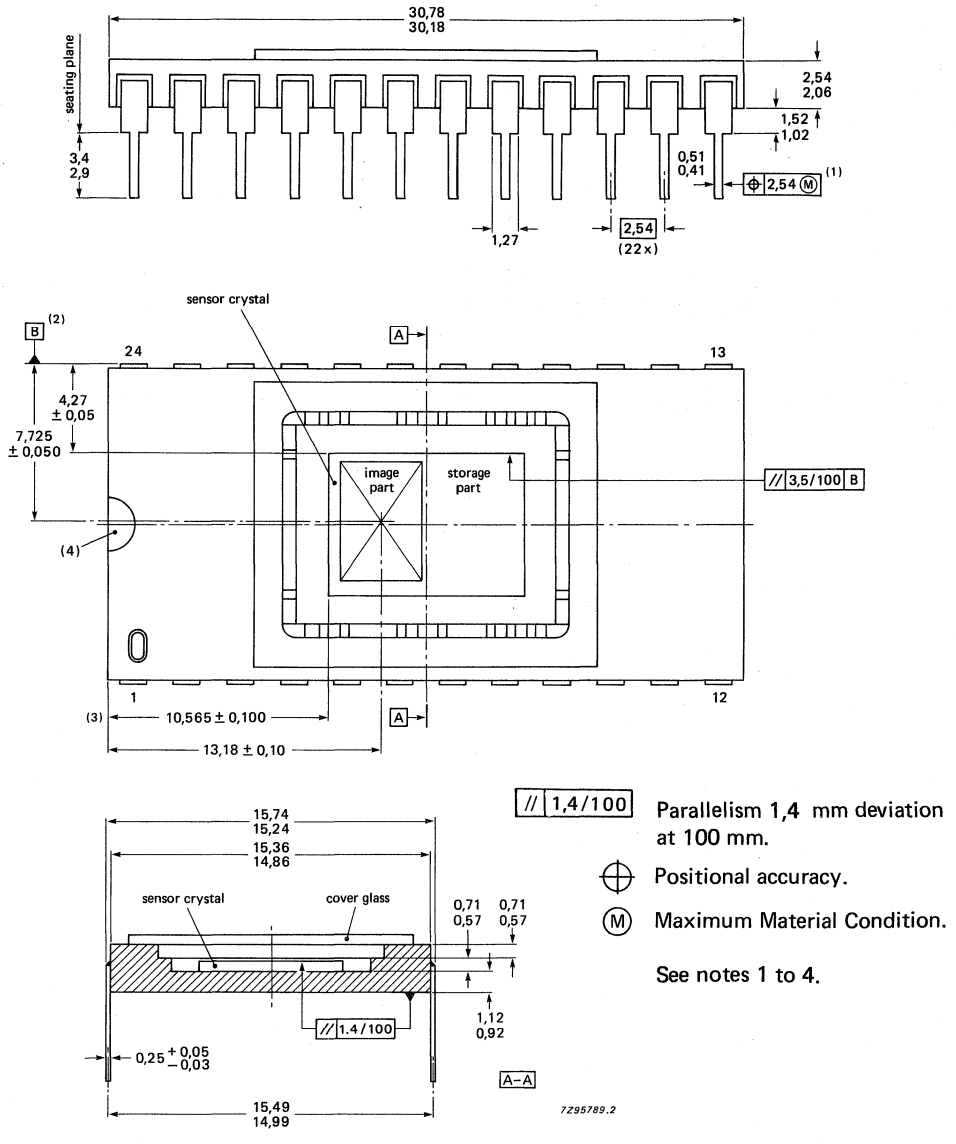


Fig. 16 Package outline; dimensions in mm.

Notes to Fig. 16

1. Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.
2. Line B is the connection line between pins 13 and 24. Pins 14 to 23 are not necessarily exactly on this line.
3. These two dimensions are measured at the centre-line of the package.
4. The gold plateau is internally connected to N_{sub}.

GENERAL DIMENSIONS (See Fig. 16)

Chip thickness	525 ± 15 μm
Cover glass thickness	550 ± 50 μm
Thickness of glue layer between sensor and cavity bottom	80 ± 30 μm
Refractive index	1,5
Transmission (400-700 nm)	90%

Sensor is filled with nitrogen.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or Wave

The maximum permissable temperature of the solder is 260 °C, this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the seating plane but the temperature of the ceramic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

APPLICATION INFORMATION

Figure 17 shows a circuit for providing the pulse sequences needed to drive the sensor. A SAA1043 sync-pulse generator provides the three TV standards, namely PAL, SECAM and NTSC. These include vertical and horizontal blanking, and black-level clamping. It also provides other signals essential for tv camera operation and can be triggered externally for operation with, for example, a VCR or computer. The sync-pulse generator drives a SAD1019 multi-norm pulse-pattern generator (MNPPG) developed specifically for the image sensors. It provides all the clock signals except the pulses for the horizontal read-out registers. Its use avoids the need to develop complex circuitry for driving the NXA1031. Fast clock pulses for the three horizontal read-out registers are generated by a horizontal clock generator. The three 3.90 MHz pulse trains generated differ in phase by 120°. The output levels from the MNPPG are too low to drive the shift registers directly, therefore, additional vertical driver IC's (VDR) TDA4301 are required to boost these signals to suitable levels. During the horizontal blanking period, slow pulses derived from the MNPPG need to be applied to the horizontal registers to sort the charge packets into the three horizontal read out registers.

More detailed information is available on request.

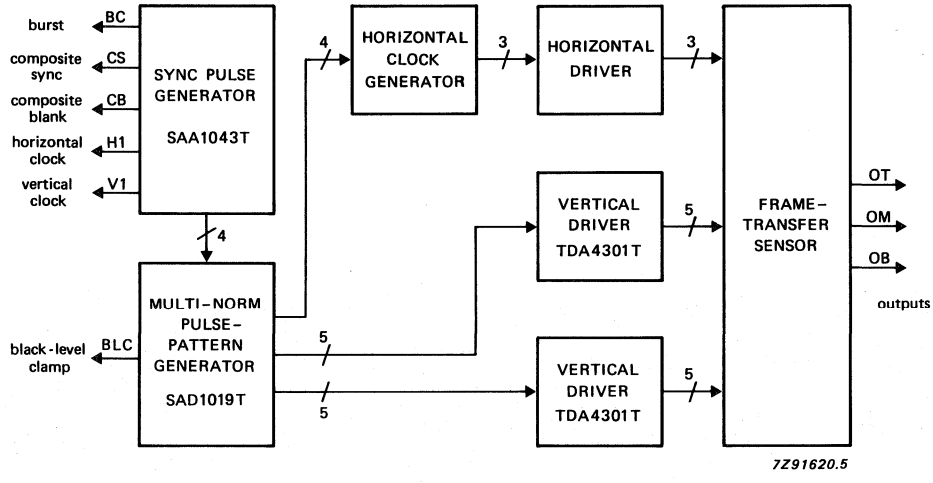


Fig. 17 Drive circuit for the NXA1031 frame transfer sensor.

FRAME TRANSFER SENSOR

GENERAL DESCRIPTION

The NXA1041 frame transfer sensor is a solid state imaging device which produces two interlaced 251-line fields (including 6 lines for dark reference and testing) with an aspect ratio of 4:3.
The sensor is equipped with an on-chip colour stripe filter. The device is compatible with NTSC TV standards and has a 7,5 mm image diagonal matching the half-inch camera tube format.

APPLICATIONS

- Consumer entertainment cameras
- Surveillance cameras – solid state reliability, high resolution and sensitivity provide the quality to be an ideal successor for your stripe camera tube
- Visual aids – the low voltage and mechanical ruggedness of this device allows design of safe and reliable cameras for visual aids
- Slide and film scanners for consumer applications

FEATURES

- Effective number of elements: 610 (horizontal) x 490 (vertical)
- Cyan, green, yellow stripe filter on the chip
- Dark reference: 1 line per field for black clamping
- 100 x anti-blooming margin
- Gamma is 1
- High sensitivity, low noise
- Freedom from lag, burn-in, geometrical distortion and microphonic noise

DEVICE ORGANIZATION

- Frame transfer charge coupled device
- Unit cell size: 9,9 μm (horizontal) x 18,6 μm (vertical)
- Separate outputs for the cyan, green, and yellow channels
- Dummy elements: the first 5 elements of the 3 output registers are dummy elements
- On-chip high sensitivity output amplifier
- Image area: 6,0 mm (horizontal) x 4,5 mm (vertical)
- Chip size: 6,95 mm (horizontal) x 9,35 mm (vertical)

FUNCTIONAL DESCRIPTION

The special electrode arrangement allows 35% of the photosensitive element to be free of polysilicon. This facilitates easy penetration of the blue light into the element to provide good blue sensitivity.

The layout of the sensor is shown in Fig. 1.
It comprises 3 functional areas:

- a matrix of photosensitive elements and integration electrodes,
- a storage section,
- three BCCD read-out registers.

Figure 2 shows the transport process in the imaging and storage regions. At time t_0, the start of the first field read-out from the imaging region, ϕ_3 is low and the charge is concentrated beneath ϕ_4 to ϕ_2. At t_1, ϕ_4 goes low and the charge in each pixel concentrates beneath ϕ_1 and ϕ_2. At t_2, ϕ_3 goes high and the charge packets advance one gate electrode, spreading out beneath ϕ_1, ϕ_2 and the following electrode ϕ_3. In the next step, at t_3, ϕ_1 goes low compressing the charge packets beneath ϕ_2 and ϕ_3, and at t_4, ϕ_4 goes high allowing the charge packets again to advance one gate electrode. This process continues in both the imaging and storage regions until all the charge packets have transferred to the storage region.

The sensor in the integration mode is shown in Fig. 3. The first field is generated when phases ϕ_4, ϕ_1 and ϕ_2 are high and ϕ_3 is low, Fig. 3(a). ϕ_3 effectively forms a potential barrier separating the pixels in the first field. The charges generated by incident light then integrate beneath ϕ_4 and ϕ_2, centred on ϕ_1. So each pixel extends vertically over four gate electrodes.
The potential distribution of the second field, and hence its position relative to the first field is shown in Fig. 3(b). The second field is always displaced by two gate electrodes relative to the first field, with its charge patterns centred on ϕ_3, and with ϕ_1 forming the barrier between pixels, thus providing a perfectly interlaced frame structure.

CAUTION

The image sensor is a MOS device which can be destroyed by static charging of the gates. Always store the device with short-circuiting clamps or on conductive foam plastic. When cleaning the glass window only use alcohol or acetone. Rub the window carefully and slowly. Dry rubbing of the window may cause static charges which can destroy the device.

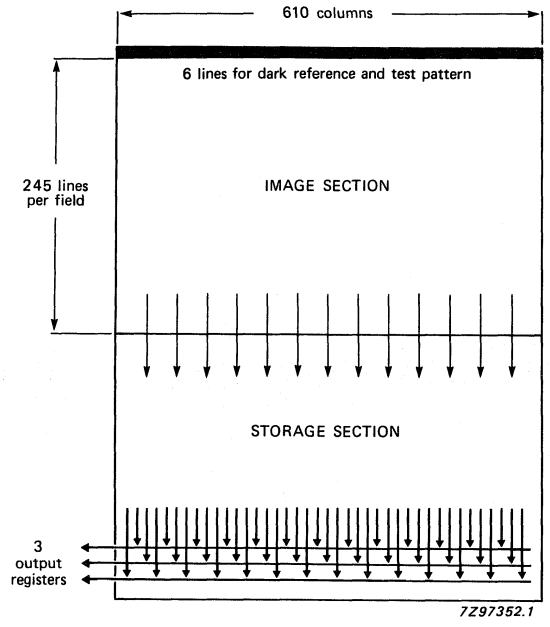


Fig. 1 Sensor layout and charge transport direction.

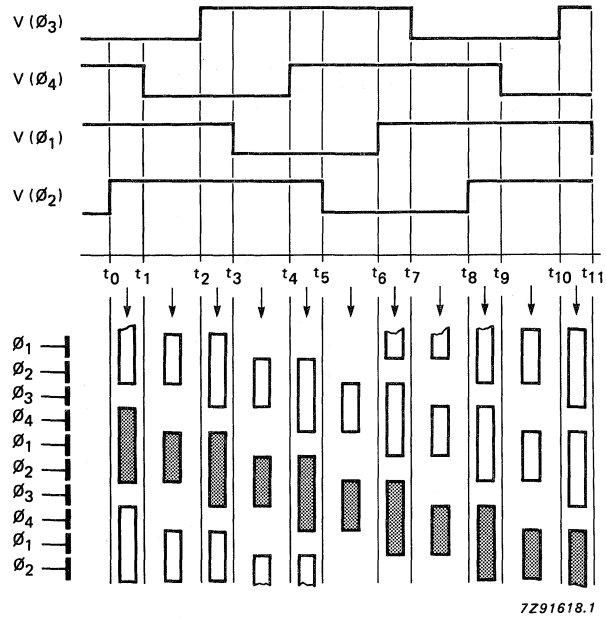


Fig. 2 Charge transport in the vertical direction.

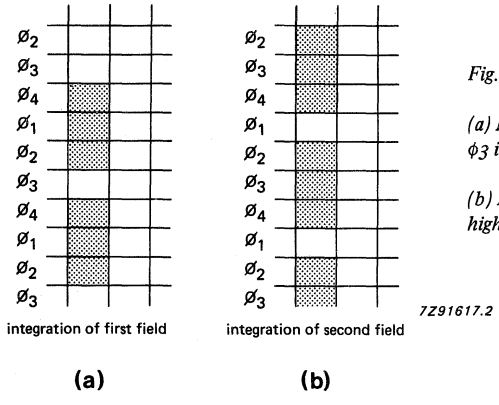


Fig. 3 Interlacing of the sensor.

(a) For integration of the first field, $\phi 4$ to $\phi 2$ are high, $\phi 3$ is low forming a barrier between charge packets.

(b) For integration of the second field, $\phi 2$ to $\phi 4$ are high, $\phi 1$ is low.

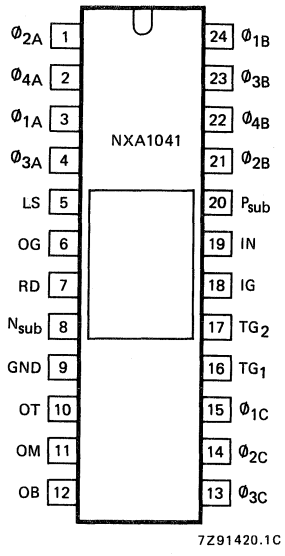


Fig. 4 Pin configuration.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	ϕ2A	Vertical transfer clocks for image part
2	ϕ4A	
3	ϕ1A	
4	ϕ3A	
5	LS	Light shield (Al. cover on storage part)
6	OG	Output gate
7	RD	Drain reset transistor
8	N_{sub}	N-substrate; supply voltage
9	GND	Ground
10	OT	Output top (cyan)
11	OM	Output middle (green)
12	OB	Output bottom (yellow)
13	ϕ3C	Horizontal transfer clock for output register
14	ϕ2C	
15	ϕ1C	
16	TG1	Transfer gate
17	TG2	
18	IG	Input gate (test point for manufacturing)
19	IN	Input diffusion (test point for manufacturing)
20	P_{sub}	P-substrate
21	ϕ2B	Vertical transfer clocks for storage part
22	ϕ4B	
23	ϕ3B	
24	ϕ1B	

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Voltages with respect to P_{sub}				
RD	$V_{RD-PSUB}$	−0,5	+25	V
IN	$V_{IN-PSUB}$	−0,5	+25	V
Voltages with respect to N_{sub}				
RD	$V_{RD-NSUB}$	−10	+0,5	V
IN	$V_{IN-NSUB}$	−10	+0,5	V
all other connections		−25	+0,5	V
Current from one output		−	10	mA
Storage temperature range	T_{stg}	−55	+80	°C
Operating ambient temperature range	T_{amb}	−40	+60	°C

DC CHARACTERISTICS at T_{amb} = 60 °C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Voltage at LS	V_{LS}	−	V_{Nsub}	−	V
Voltage at OG (note 1)	V_{OG}	4	−	7	V
Voltage at RD; current to sensor: $I < 1\ \mu A$	V_{RD}	15,5	16	16,5	V
Voltage at N_{sub}; $I < 10$ mA	V_{Nsub}	19,5	20	20,5	V
Voltage at IG	V_{IG}	−	GND	−	V
DC level of output voltage at OT, OM, OB (notes 2 and 3)	$V_{OT; OM; OB}$	6	−	15	V
Voltage at P_{sub}; (note 1) current from sensor: $I < 50\ \mu A$	V_{Psub}	2	−	5	V
Voltage at IN	V_{IN}	−	V_{Nsub}	−	V
Power dissipation	P	−	80	150	mW
Leakage current of gates	I_I	−	−	2.5	μA

Notes

1. These values must be adjusted to the optimum operating point within the given range.
2. Measured with output buffer. See Fig. 5.
3. See Fig. 16.

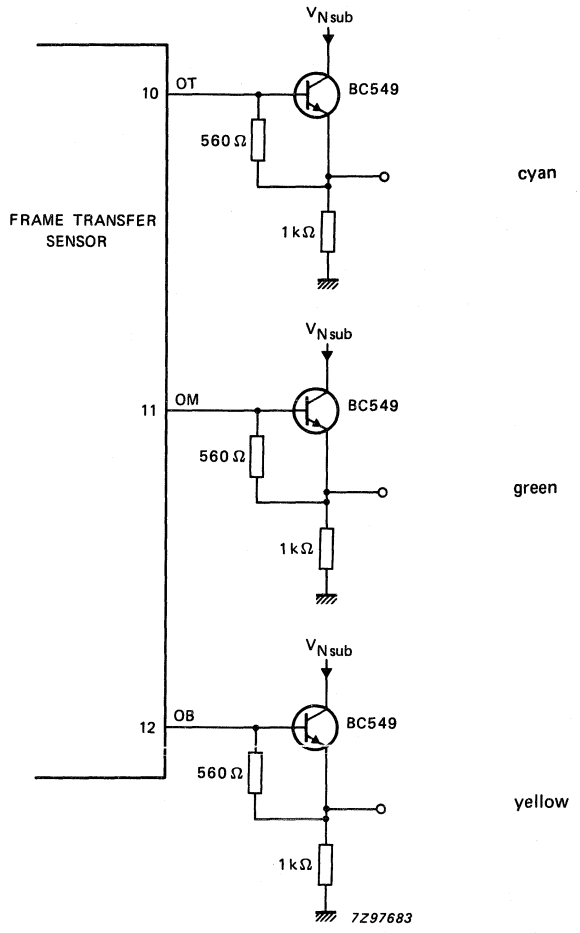


Fig. 5 Output buffer for measurements.

CLOCK CHARACTERISTICS (note 1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
LOW levels					
ϕnA, ϕnB	$V_{\phi nA/B}$	–	GND	–	–
ϕ1C, ϕ2C, ϕ3C (ϕ1CLOW = ϕ2CLOW = ϕ3CLOW) (note 2)	$V_{\phi nC}$	0	3,5	5	V
TG1 (note 2)	V_{TG1}	0	1	4	V
TG2 (note 2)	V_{TG2}	0	6,5	8	V
Amplitudes					
ϕnA, ϕnB, ϕnC	$V_{\phi(p-p)}$	9,75	10	10,25	V
Timing (see Figs 6 and 7)					
Horizontal clocks					
clock frequency (note 3)	f_c	–	3,90	–	MHz
rise time	t_{rc}	20	–	40	ns
fall time	t_{fc}	20	–	40	ns
overlap time	t_{ihc}	10	–	–	ns
	t_{ilc}	5	–	–	ns
Vertical clocks					
clock frequency	f_{cv}	–	629	–	kHz
rise time	t_{rv}	–	50	–	ns
fall time	t_{fv}	–	70	–	ns
overlap time	t_{ihv}	80	100	120	ns
	t_{ilv}	100	200	260	ns
Transfer gates					
rise time	t_{rTG}	–	70	–	ns
fall time	t_{fTG}	–	100	–	ns
Clock capacitance					
Each clock phase ϕnA, ϕnB	$C_{\phi nA/B}$	–	–	3000	pF
ϕnC, TG1, TG2	$C_{\phi nC}$, $C_{TG1/2}$	–	–	100	pF
Leakage current of the clock connections	I_l	–	–	2,5	μA

Notes

1. Measured with output buffer. See Fig. 5.
2. These values must be adjusted to the optimum operating point within the given range.
3. Deviations from this frequency result in incorrect aspect ratio.

ADJUSTMENT OF OPERATING LEVELS

For optimum performance, fine adjustment of the sensors DC levels is essential. When carrying out this operation the following points should be considered.

- Vertical stripes in the picture are usually the result of charges being unevenly sorted into the three output registers. This can be influenced by offsets $V_{\phi C}$, V_{TG1}, V_{TG2} and V_{OG}.
- The anti-blooming performance of a sensor is influenced by its internal vertical potential gradient. This can be optimized by adjusting V_{Psub}.

DRIVING PULSE WAVEFORMS

The specifications of the sensor are measured when the following clock pulses are applied (Figs 6 and 7). In principle the sensor can be operated with different clock pulses, e.g. different clock frequencies (overlap conditions have to be maintained).

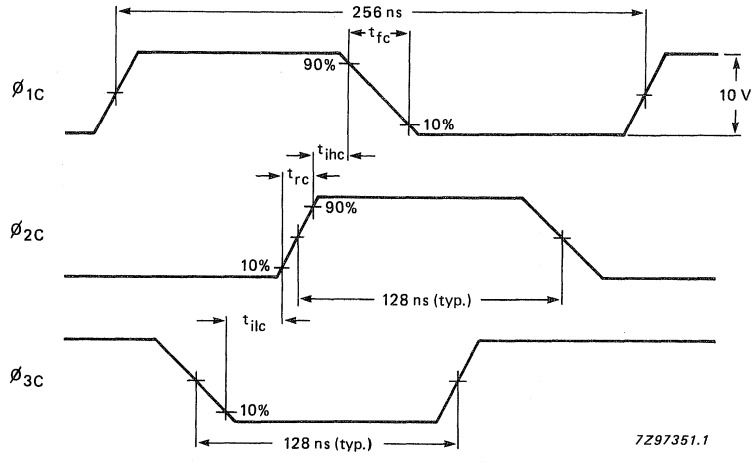


Fig. 6 Horizontal transport timing waveforms for the sensor electrodes (ϕ_{nC}); times measured at the 10% and 90% points of the amplitude.

DRIVING PULSE WAVEFORMS (continued)

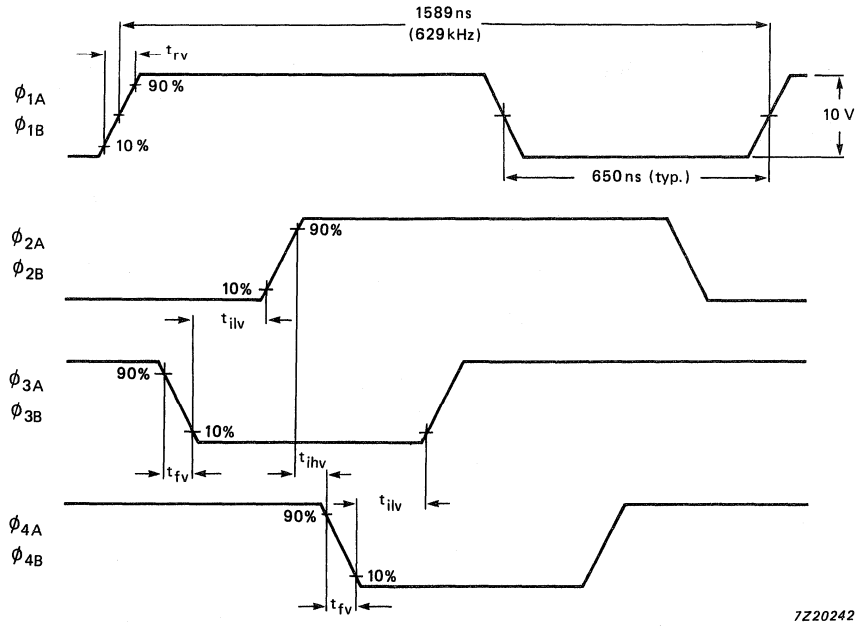


Fig. 7 Vertical transport timing waveforms for the sensor electrodes (ϕ_{nA}, ϕ_{nB}); times measured at the 10% and 90% points of the amplitude.

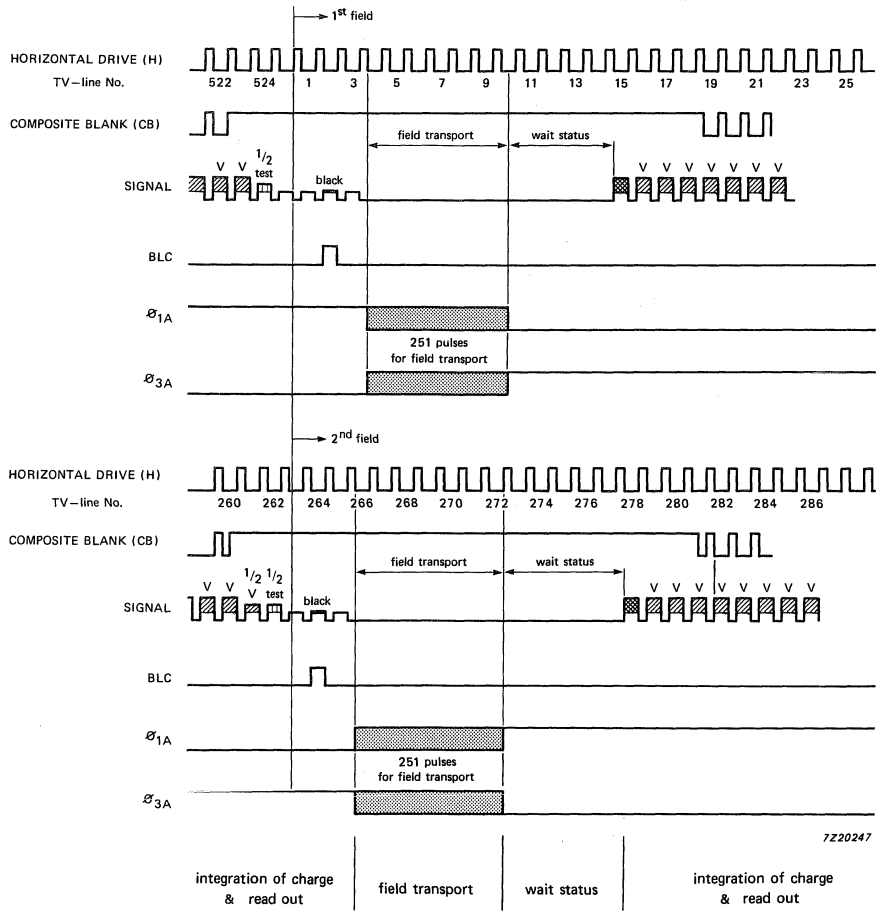


Fig. 8 Drive-pulse sequence and line numbering for field transport.

DEVELOPMENT DATA

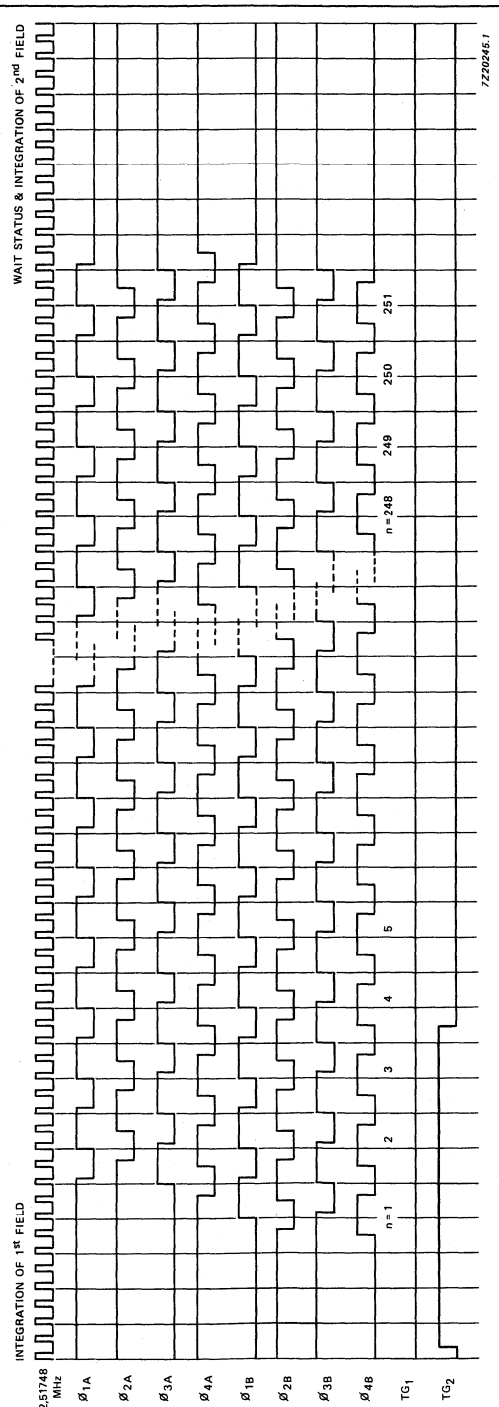


Fig. 9 Field transport pulses 1st field.

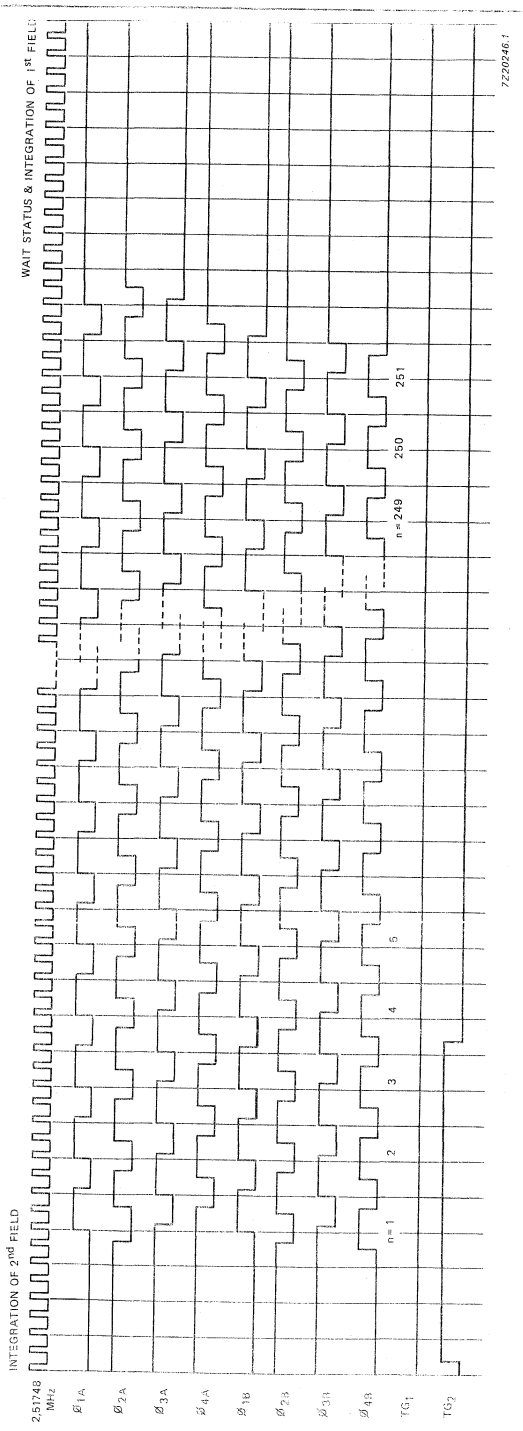


Fig. 10 Field transport pulses 2nd field.

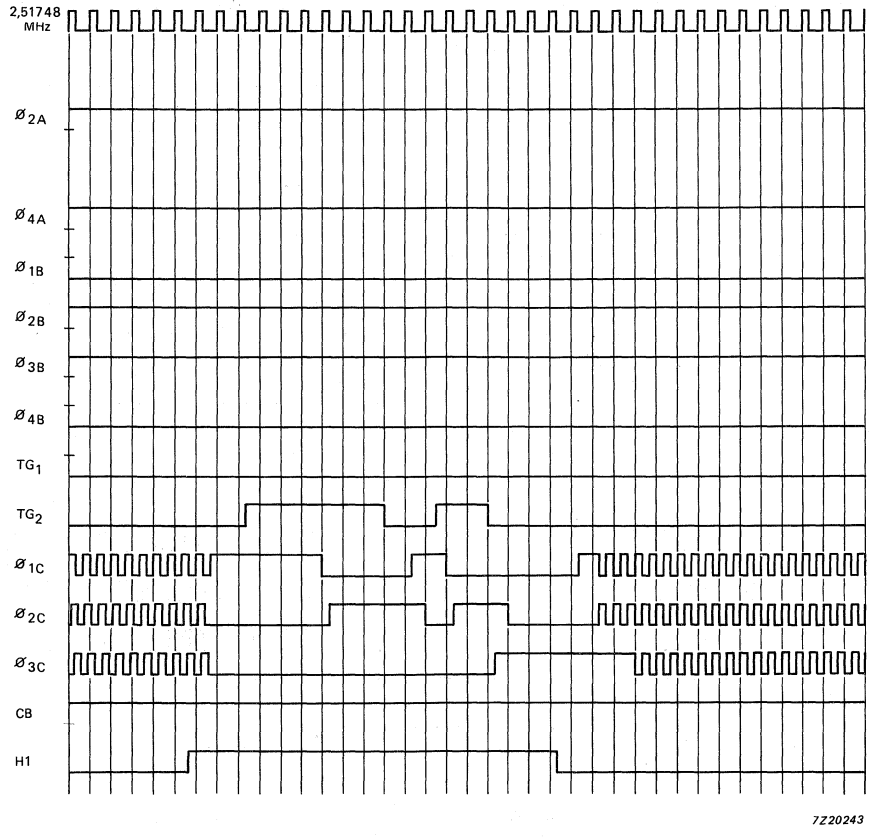


Fig. 11 Wait status.

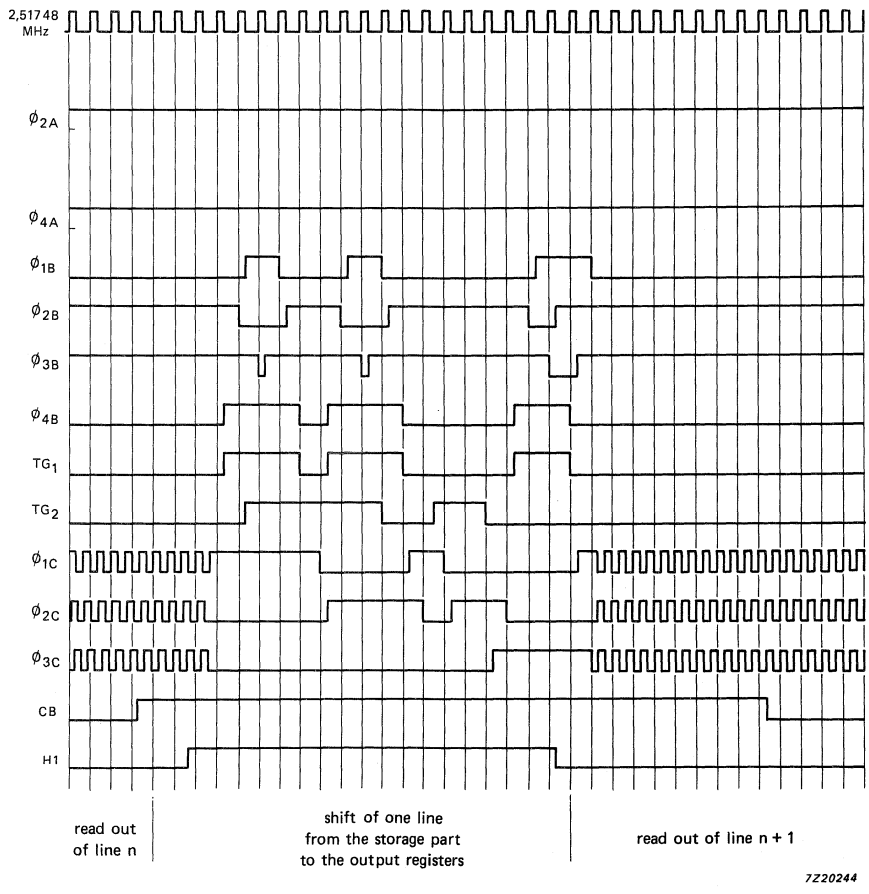


Fig. 12 Read-out of the output registers and sorting of the signal into output registers.

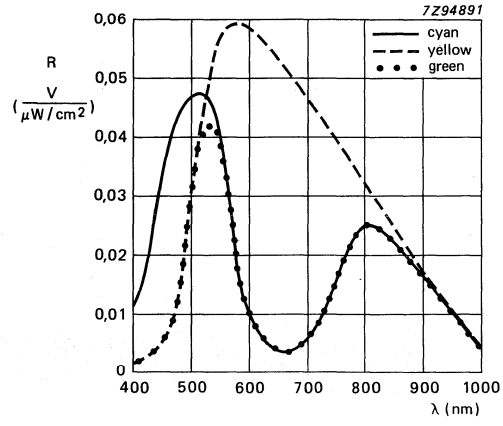


Fig. 13 Spectral response.

OUTPUT CHARACTERISTICS at T_{amb} = 60 °C

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Load capacitance	C_L	–	–	10	pF
Output signal voltage at standard illumination (peak-to-peak value) (see notes 1 and 2)					
Cyan channel	V_{OT}	30	–	–	mV
Green channel	V_{OM}	27	–	–	mV
Yellow channel	V_{OB}	60	–	–	mV
Output signal voltage at saturation (peak-to-peak value) (note 2)	V_{Osat}	300	600	1200	mV
Maximum illumination on the sensor without blooming (note 3)	E_B	2000	–	–	lx
Transport inefficiency					
horizontal one step	ϵ_H	–	–	$8{,}5 \times 10^{-5}$	
vertical one step	ϵ_V	–	–	5×10^{-5}	
Dark current	I_D	–	–	3	nA
Smear (note 4)					%

Notes

1. 5 lx on the sensor, colour temperature of light source 3200 K, Hoya-IR-Filter C500S, 1 mm is used.
2. Measured with output buffer.
3. See 'Defenition of blooming'.
4. See 'Defenition of smear'.

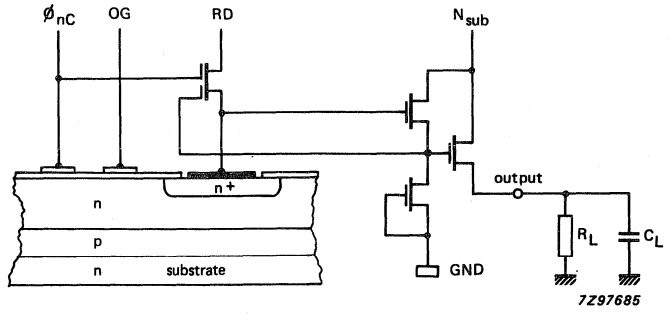


Fig. 14 Circuit diagram for one output channel.

DEFINITION OF SMEAR

During the field transport time the complete field is shifted over the image section. So each pixel of one column is illuminated by the light on all the other pixels of one column for a short time. Therefore a bright spot makes a bright vertical stripe on the image. This effect is called smear. The brightness of the stripe depends on the height of the spot and on the illumination of the spot.

It is defined by the equation:

$$V_{smear} = \frac{t_{field\ transport}}{t_{integration}} \times \frac{h}{H} \times \frac{E}{E_{sat}} \times V_{sat}$$

Where:

V_{smear} = Additional output voltage due to smear
$t_{field\ transport}$ = 0,4 ms
$t_{integration}$ = 16,2 ms
h = Height of bright spot
H = Height of the complete image
E = Illumination of the spot
E_{sat} = Saturation illumination
V_{sat} = Output voltage at saturation

Example:

Spot height is 10% of the height.
Spot illumination is 100% of saturation.

$$V_{smear} = \frac{0,4}{16,2} \times 0,1 \times 1 \times V_{sat} = 0,0024 \times V_{sat}$$

DEFINITION OF BLOOMING

When part of the image section (spot) is illuminated above saturation level and with the rest of the image dark, at a certain level of overexposure (2000 lx for the NXA1041), the area of the spot increases irregularly. This effect is called blooming.

PICTURE ELEMENT DEFECTS

picture quality at T_{amb} = 60 °C

GRADE	PIXEL DEFECTS (note 1)	CLUSTERS (note 2)	COLUMN DEFECTS (note 3)
01	0	0	0
02	2	0	0
03	10	2	0
04	35	5	2

Notes

1. A picture element is considered defect, if its signal deviates more than ±10% from the mean signal of the neighbouring picture element at standard illumination.
2. A cluster is a pair of two defect pixels at a distance of less than 3% of the picture height. The sum of pixel defects and clustered pixel defects does not exceed the number of permitted pixel defects. A pixel defect in the same place in odd and even fields is not defined as a cluster.
3. If more than two pixel defects occur in one column, this is considered a column defect. Additionally the indicated number of defect pixels is allowed.

OUTPUT SIGNAL

The output signal is a pulse sequence with a DC offset. The HIGH level of the output pulses, dependent upon the DC adjustments, varies between 6 and 15 volts. The LOW levels depend upon the signal voltage, itself a function of the intensity of the light falling on the sensor, and is between 1.0 and 0.2 volts below the HIGH level. These pulses contain the video information and need further processing to be converted into a signal suitable for use in standard video circuitry.

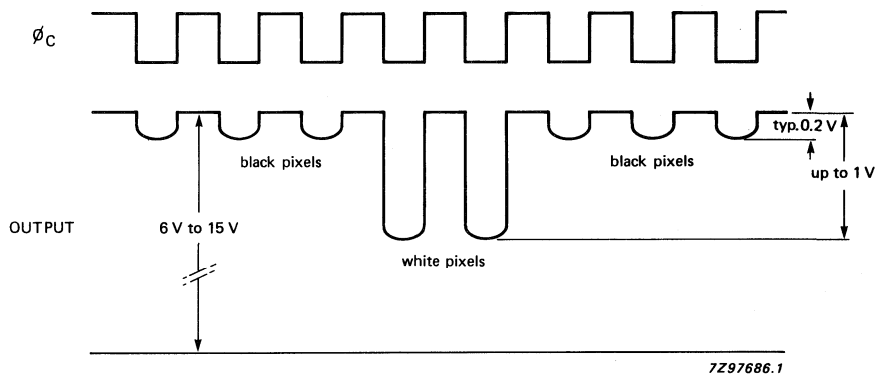


Fig. 15 Typical signal at the sensor output.

MECHANICAL PARAMETERS

The sensor is encapsulated in a 24-lead dual in-line ceramic package with a high-quality glass viewing window on the top side for admittance of light to the sensor.

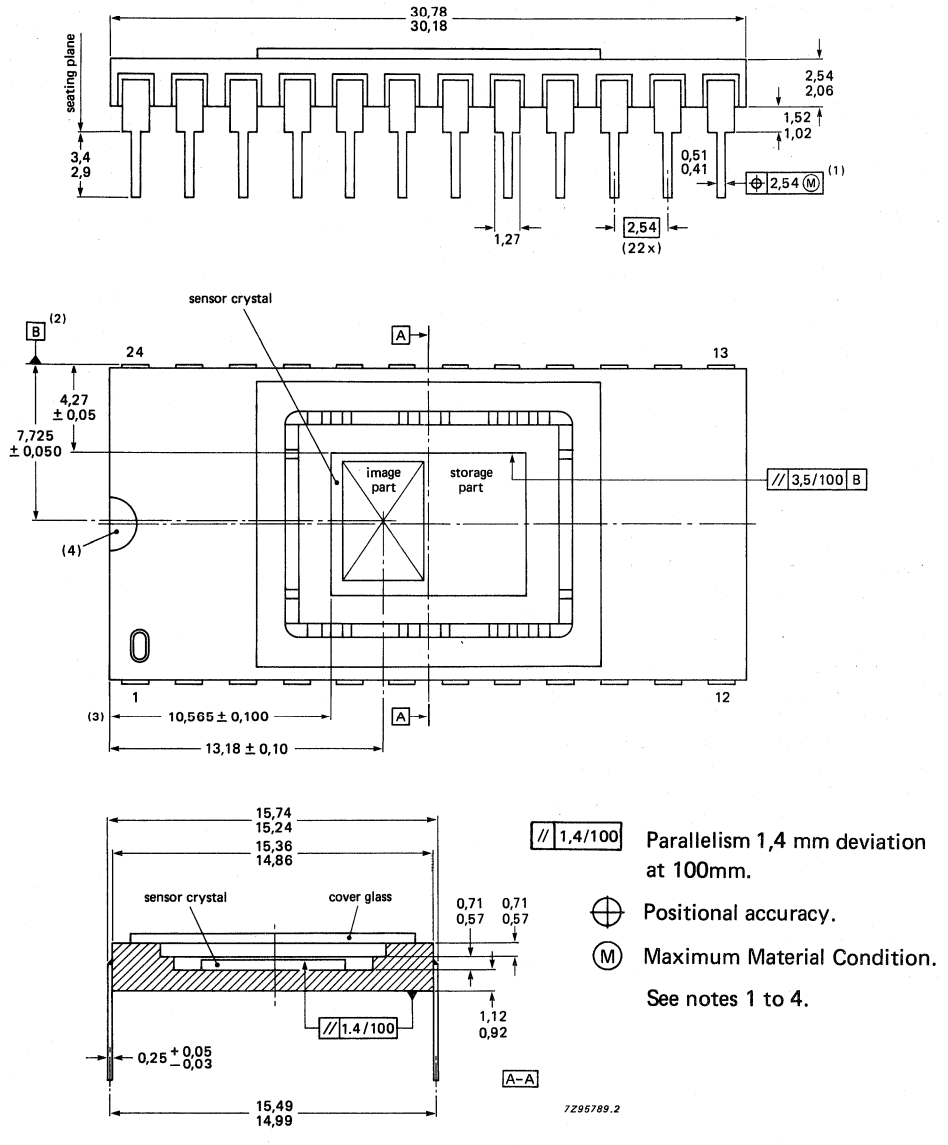


Fig. 16 Package outline; dimensions in mm (also see notes).

Notes to Fig. 16

1. Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.
2. Line B is the connection line between pins 13 and 24. Pins 14 to 23 are not necessarily exactly on this line.
3. These two dimensions are measured at the centre-line of the package.
4. The gold plateau is internally connected to N_{sub}.

GENERAL DIMENSIONS (See Fig. 16)

Chip thickness	525 ± 15 μm
Cover glass thickness	550 ± 50 μm
Thickness of glue layer between sensor and cavity bottom	80 ± 30 μm
Refractive index	1,5
Transmission (400-700 nm)	90%

Sensor is filled with nitrogen.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or Wave

The maximum permissable temperature of the solder is 260 °C, this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds. The device may be mounted up to the seating plane but the temperature of the ceramic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

APPLICATION INFORMATION

Figure 17 shows a circuit for providing the pulse sequences needed to drive the sensor. A SAA1043 sync-pulse generator provides the three TV standards, namely PAL, SECAM and NTSC. These include vertical and horizontal blanking, and black-level clamping. It also provides other signals essential for tv camera operation and can be triggered externally for operation with, for example, a VCR or computer. The sync-pulse generator drives a SAD1019 multi-norm pulse-pattern generator (MNPPG) developed specifically for the image sensors. It provides all the clock signals except the pulses for the horizontal read-out registers. Its use avoids the need to develop complex circuitry for driving the NXA1041. Fast clock pulses for the three horizontal read-out registers are generated by a horizontal clock generator. The three 3.9 MHz pulse trains generated differ in phase by 120°. The output levels from the MNPPG are too low to drive the shift registers directly, therefore, additional vertical driver ICs (VDR) TDA4301 are required to boost these signals to suitable levels. During the horizontal blanking period, slow pulses derived from the MNPPG need to be applied to the horizontal registers to sort the charge packets into the three horizontal read out registers.

More detailed information is available on request.

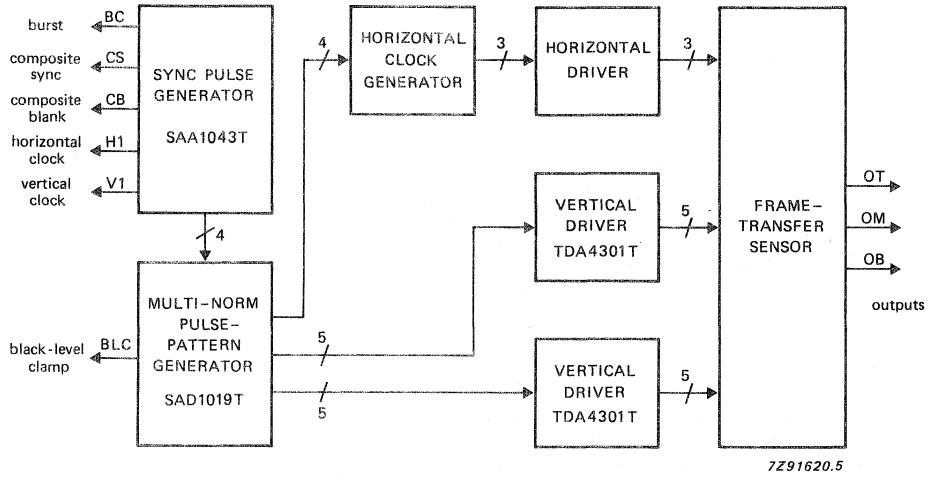


Fig. 17 Drive circuit for the NXA1041 frame transfer sensor.

MONOCHROME IMAGING MODULE

INTRODUCTION

The 5647X monochrome imaging module is a compact imaging unit requiring only a lens and case to form a complete solid state monochrome TV camera or character recognition system. The module is built around a CCD frame transfer image sensor and consists of five printed circuit boards (PCBs) which contain all the circuitry necessary for a high quality, fully interlaced TV camera. The modules are available for CCIA and EIA TV standards and each are graded according to the quality of the sensor used (see Table 1). System standards can use free-running, internal or external synchronization.

Table 1 Type numbers

module no.	TV standard	sensor/grade*
56470	CCIR	NXA1011/01
56471	EIA	NXA1031/01
56472	CCIR	NXA1011/02
56473	EIA	NXA1031/02
56474	CCIR	NXA1011/03
56475	EIA	NXA1031/03

* See "Technical Specification" for grading system.

Functionally, the module can be divided into five parts on five separate PCBs:

- master timing and sensor drive circuitry
- sensor with buffering circuitry and rigid lens mount
- signal pre-processing including adjustment circuitry
- video (post-) processing
- power supply

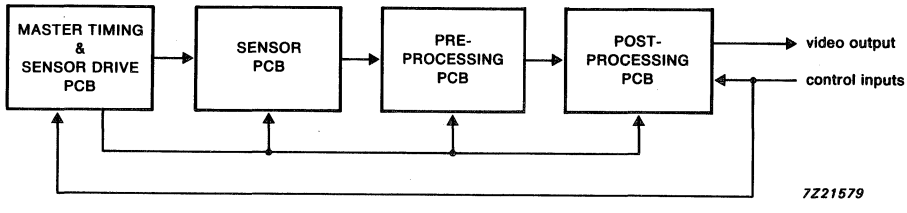


Fig.1 The monochrome imaging module (power supply not shown).

SPECIFICATIONS

Measured at 25 °C with recommended power supply

Sensor grades	/01	/02	/03
Pixel defects	0	max. 2	max. 10
Cluster defects	0	0	max. 2
Column defects	0	0	0
	NXA1011	**NXA1031**	
TV standard	CCIR-B	EIA	
Number of pixels			
Interlaced	604 x 588	610 x 488	
Progressive scan	604 x 294	610 x 244	
Image area	6 x 4.5	6 x 4.5	mm
Resolution	min. 450	min. 450	TV lines
Bandwidth (–6 dB)	5.8	5.8	MHz
Geometric distortion	0	0	
Sensor illumination			
For picture acceptability	min. 0.02	min. 0.02	lx
For –6 dB output	min. 0.05	min. 0.05	lx
Signal-to-noise ratio weighted at 5 lx illumination, AGC off, gamma off	min. 46	min. 46	dB
Gamma correction (switchable)	0.45 or 1	0.45 or 1	
Video output (peak-to-peak)			
Composite video (75 Ω load)	1	1	V
Iris control (> 10 kΩ load)	1	1	V
Gain control			
Input open-circuit	AGC selected	AGC selected	
External DC control voltage	0 to 11	0 to 11	V
Supply voltage (+ 10%, –2%)	12	12	V
Power consumption	2	2	W
Lens mount	1/2" C-mount	1/2" C-mount	
Mass	95	95	g

RATINGS

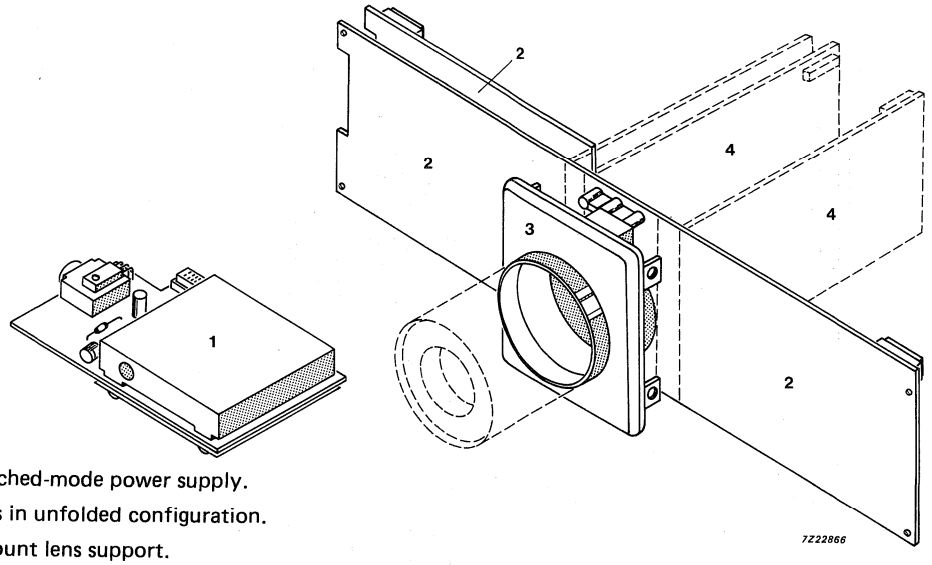
Limiting values in accordance with the Absolute Maximum System (IEC 134)

	min.	max.	
Operating voltage, DC	11.78	13.2	V
Operating temperature	–10	50	°C
Storage temperature	–20	70	°C

ENVIRONMENTAL

All tests were conducted at 60 to 100 kPa pressure and 20 to 95 relative humidity with the module housed in the recommended casing.

Operating limits	–10 to + 50 °C
Performance to spec	0 to 40 °C
Humidity (40 °C, 21 days)	IEC 68-2-30, test Db
Vibration (amplitude 0.15 mm, 10 to 50 Hz)	IEC 68-2-6, test Fc
Shock (3 shocks in each direction, 60 g)	IEC 68-2-27, test Ea
Bump (1000 bumps 3 times, 10 g)	IEC 68-2-29, test Eb
RF interface requirements	CENELEC/CISPR, cat. II and VDE871 class B



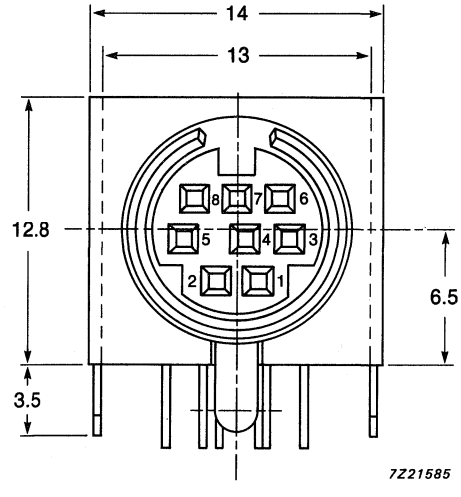
1. Switched-mode power supply.
2. PCBs in unfolded configuration.
3. C-mount lens support.
4. PCBs in folded configuration.

Fig.2 CCD module showing both ways of mounting.

External connections

The connector (female) is on the video (post- processing) PCB:

pin 1: power ground
pin 2: signal ground
pin 3: scan-mode input (open = CCIR & EIA interlaced, grounded = CCIR progressive-scan, +5 V = EIA progressive-scan)
pin 4: gamma-on/off input (open = gamma off, grounded = gamma on (0.45))
pin 5: power supply input (+ 12 V DC)
pin 6: external sync input (200 mV_{p-p} to TTL level
pin 7: video output (1 V_{p-p} into 75 Ω)
pin 8: manual gain control input (open = off, 0 to 11 V for increasing gain).



Dimensions in mm

Fig.3 The 8-pole mini-DIN connector is the interface between the module and the outside world.

The 3.5 mm stereo jack connector is the iris-control output. It is on the power supply PCB and is wired as follows:

body: ground for signal and lens power supply
ring: iris-control (video) output
tip: lens power supply (11.5 V)

Dimensions in mm

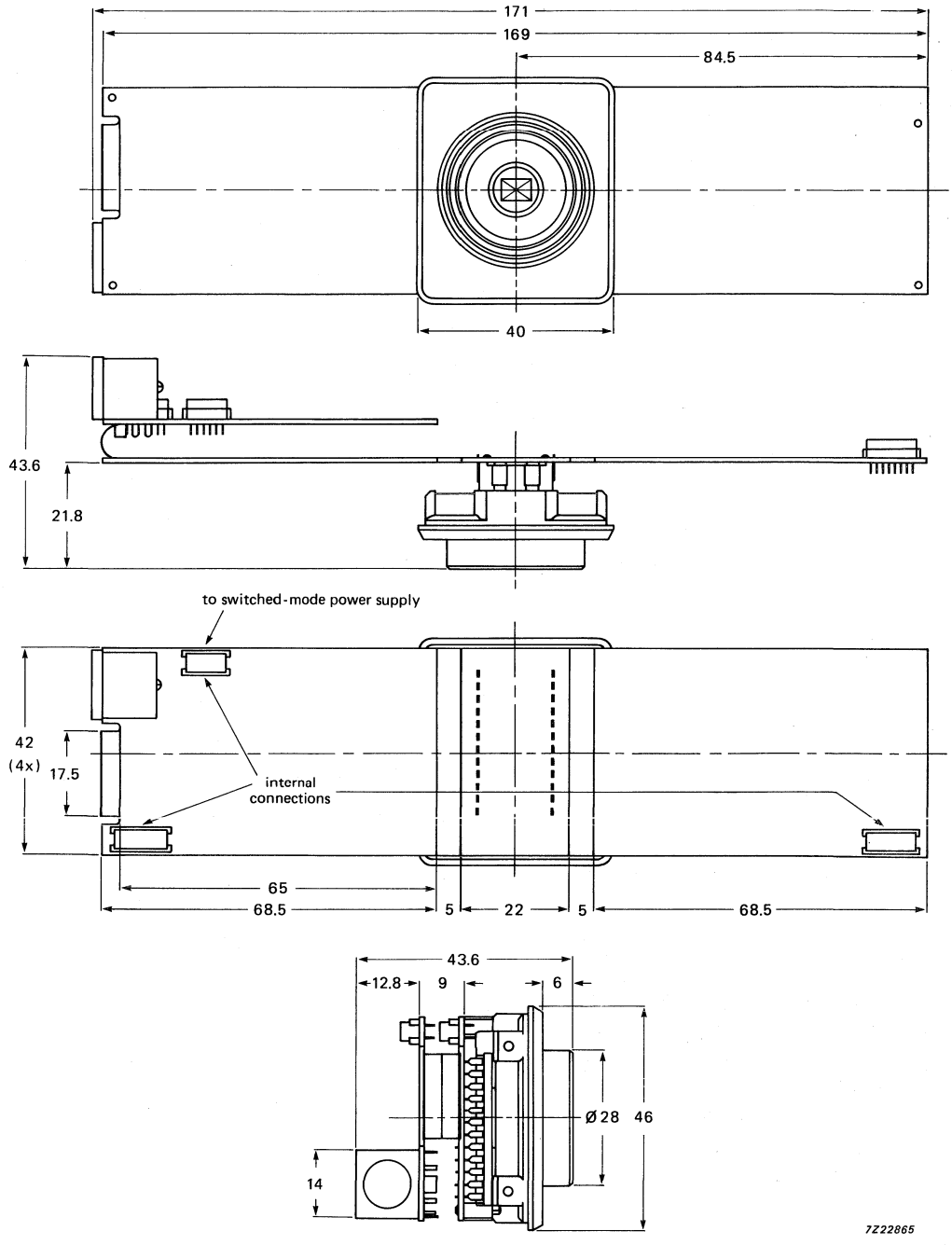


Fig.4 Mechanical outline.

Peripheral Sensor Driving ICs

UNIVERSAL SYNC GENERATOR

GENERAL DESCRIPTION

The SAA1043 generates the synchronizing waveforms required in all types of video source equipment (video cameras, film-scanners, video games, computer displays and similar applications). The device is programmable to suit standards SECAM1, SECAM2, PAL/CCIR, NTSC1, NTSC2 and PAL-M; the video game 624 and 524-line standards; and can be synchronized to an external sync signal. Inputs and outputs are CMOS compatible.

Features

- Programmable to eight standards
- Horizontal frequency manipulation for application in non-standard systems
- Oscillator functions with LC or crystal elements
- Additional outputs to simplify camera signal processing
- Can be synchronized to an external sync signal
- Vertical reset for fast vertical lock
- Subcarrier lock in combination with subcarrier coupler SAA1044
- Very low power consumption

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 28)	V_{DD}	5.7	–	7.5	V
Supply current range (quiescent)	I_{DD}	–	–	10	μA
Oscillator frequency	f_{OSC}	–	–	5.1	MHz
Operating ambient temperature range	T_{amb}	−25	–	+ 70	°C

PACKAGE OUTLINES

SAA1043 : 28-lead DIL; plastic (SOT117).
SAA1043T: 28-lead mini-pack; plastic (SO28; SOT136A).

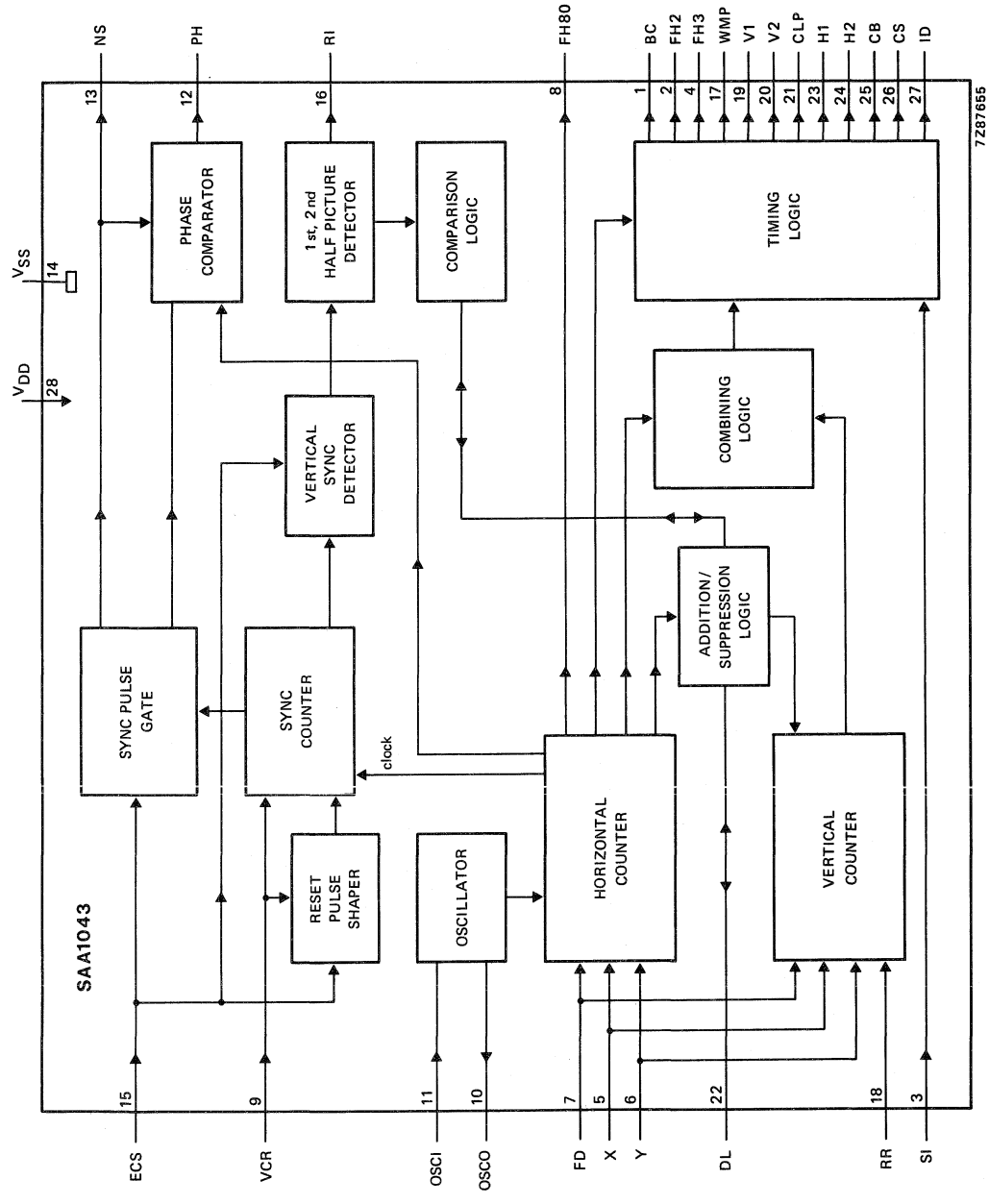


Fig. 1 Block diagram.

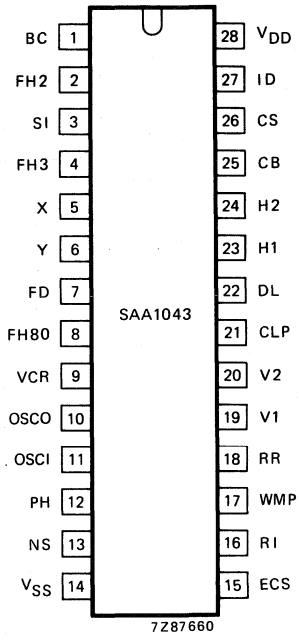


Fig. 2 Pinning diagram.

PINNING

1	BC	burst flag/chrominance blanking (SECAM) output
2	FH2	PAL identification output
3	SI	set identification input (SECAM, PAL, PAL-M)
4	FH3	400 Hz (PAL); 360 HZ (NTSC, PAL-M) and $f_H/3$ (SECAM)
5	X	standard programming input
6	Y	standard programming input
7	FD	standard programming input
8	FH80	80 x f_H output (1.25 MHz)
9	VCR	VCR standard input
10	OSCO	oscillator output
11	OSCI	oscillator input
12	PH	phase detector output
13	NS	no-sync detector output
14	V_{SS}	negative supply voltage (ground)
15	ECS	external composite sync input
16	RI	vertical identification output
17	WMP	white measurement pulse output
18	RR	vertical reset input
19	V1	vertical drive output
20	V2	vertical drive output
21	CLP	clamp pulse output
22	DL	2 x f_H input/output
23	H1	horizontal drive output
24	H2	horizontal drive output
25	CB	composite blanking output
26	CS	composite sync output
27	ID	SECAM identification output
28	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Sync pulse generation

Programming of operating standard

The standard required for operation is programmed using the inputs X, Y and FD as shown in Table 1. The FD input selects 525 or 625-line working of the vertical counter (524 or 624-lines for video game standards) and also influences the choice of oscillator frequency as shown in Table 2.

Table 1 Programming of operating standard

standard	FD	X	Y
SECAM 1	0	0	0
SECAM 2	0	0	1
624	0	1	0
PAL/CCIR	0	1	1
NTSC 1	1	0	0
NTSC 2	1	0	1
524	1	1	0
PAL-M	1	1	1

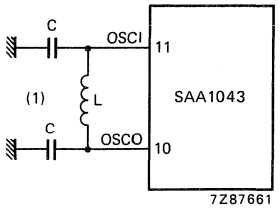
positive logic: 1 = HIGH; 0 = LOW

Oscillator

The built-in oscillator of the SAA1043 functions with an external LC-circuit (Fig. 3) or with a crystal of the parallel resonance type (Fig. 4). For operation in the VCR mode the LC oscillator circuit is recommended. The frequencies required for the operating standards are shown in Table 2.

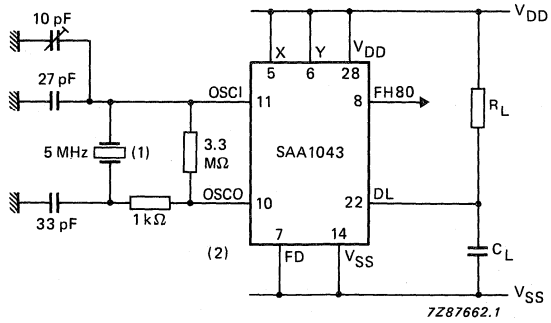
Table 2 Oscillator input frequencies

operating standard	osc. frequency (f_{OSCI}) MHz	vertical divider (FD)	vertical frequency (f_V) Hz	horizontal frequency (f_H) Hz
PAL, SECAM, 624	5.0	0	50	15625
NTSC, PAL-M, 524	5.034964	1	59.94	15734.26
PAL, SECAM, 624	2.5	H2 (pin 24)	50	15625
NTSC, PAL-M, 524	2.51782	H1 (pin 23)	59.94	15734.26



(1) Component values can be calculated from the formula $f_{OSCI} = 1/2\pi\sqrt{LC_V}$ where $C_V = C/2 + C_p$ and C_p = parasitic capacitance of typically 5 pF.

Fig. 3 LC oscillator circuit.



(1) Catalogue number of crystal: 8222 298 40760.

(2) All inputs not shown are at V_{SS}.

Fig. 4 Crystal oscillator circuit showing test set-up for oscillator frequency measurement.

Synchronization to an external sync signal

Use is made of the phase comparator output PH to lock the internally generated sync pulses to an external sync signal. Reset pulses derived at each falling edge of the external sync signal (ECS) reset the the sync counter which is clocked at the internal horizontal frequency by the horizontal counter. At each horizontal scan period the sync counter opens the sync pulse gate and allows the ECS to be applied to the phase comparator where it is compared with the phase of the internally generated horizontal sync pulse. When the two signals are in phase the output PH is in a high impedance state. When a phase difference exists PH is pulled towards V_{DD} or V_{SS} depending on the direction of the error (Fig. 5). The phase-analogue voltage on PH is used to correct the frequency at OSCI via a voltage-controlled oscillator and null the phase error between internal and external signals. Pulses occurring on the ECS outside of the sync pulse gating time (serration and equalization pulses) do not effect the phase comparator.

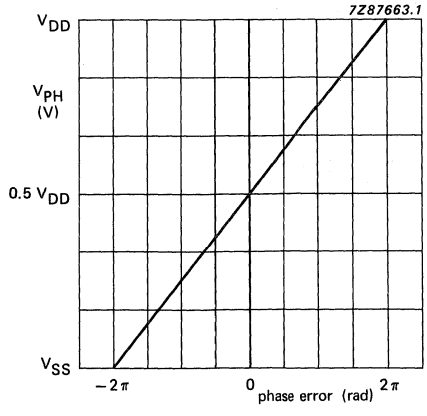


Fig. 5 Phase comparator characteristic.

FUNCTIONAL DESCRIPTION (continued)

Synchronization to an external sync signal (continued)

The circuit will lock to standard and non-standard sync signals. With standard signals the resetting of the sync counter is permitted after 3/4 of the horizontal scan period and if one reset pulse is missed the next pulse will reset the counter. With non-standard signals a narrow reset window is imposed to avoid disturbances which would otherwise be visible on the screen during vertical blanking time. The width of this window is $64 - 15.2 <$ reset time $< 64 + 15.2$ μs. If a reset pulse does not occur within this window the same window timing is specified for the next horizontal scan.

A no-sync signal is generated by the sync pulse gate if the sync counter is not reset from the ECS. The no-sync signal (NS) occurs 6.4 μs after the time of the missing reset pulse.

Detection of the vertical sync in the ECS is performed using a double sampling method which minimizes detection failures. Vertical lock is performed by comparing the internal vertical sync with a pulse derived from the ECS and using the result to modify the period of the vertical counter. This is achieved by manipulating the DL ($2 \times f_H$) input to the vertical counter via the addition/subtraction logic. The DL pulses are added or suppressed to bring the circuit into lock in the shortest possible time; the direction taken is determined by a logic decision based on the half picture in which the ECS derived pulse occurred.

Vertical reset input (RR)

The RR is used when external synchronization runs on separate vertical (V) and horizontal (H) pulses instead of composite sync (CS) pulses.

- RR = LOW : no external sync or external CS to ECS input
- RR = V-pulses: external sync with H and V requires H-pulses to ECS input
  duration of H-pulse < 5 μs
  duration of V-pulse 1 $\mu s < t_V < 3$ μs

VCR standard input (VCR)

The VCR input sets the synchronization standard for VCRs.

- VCR = HIGH: normal mode

Then the ECS input expects a 64 $\mu s \pm 16$ μs H-part of the CS pulse.
If the pulse fits inside the window, the SAA1043 will continue to take synchronizing pulses only inside the window.
If the pulse does not occur inside the window, the synchronizing circuit will take off the window and accept pulses at any time.

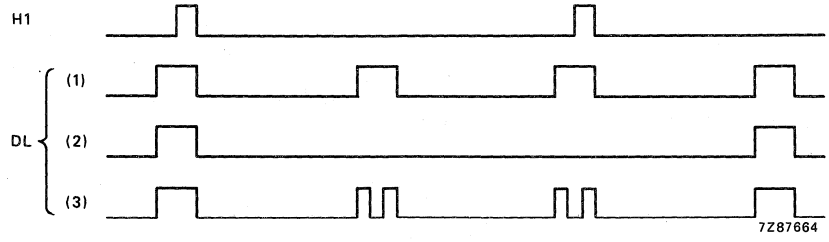
- VCR = LOW: VCR mode

The window ± 16 μs is always applied.

If the colour burst is not present in the correct position, or FH2 is not in phase with the incoming signal, the set identification input (SI) must be set to logic HIGH on line 2 for the duration of 1 line.

Use in non-standard systems

For systems requiring a non-standard horizontal frequency the number of horizontal scans per picture can be manipulated using the open drain input/output DL. The addition or suppression of pulses during the high ohmic period of DL modifies the vertical counter value. The suppression of two DL pulses per half picture will give one extra horizontal scan and the addition of two DL pulses will remove one horizontal scan from the half picture (see Fig. 6).



(1) Normal waveform at DL; $f_{DL} = 2 \times f_H$.

(2) Waveform at DL with two pulses suppressed increases the number of horizontal scans per half picture by 1.

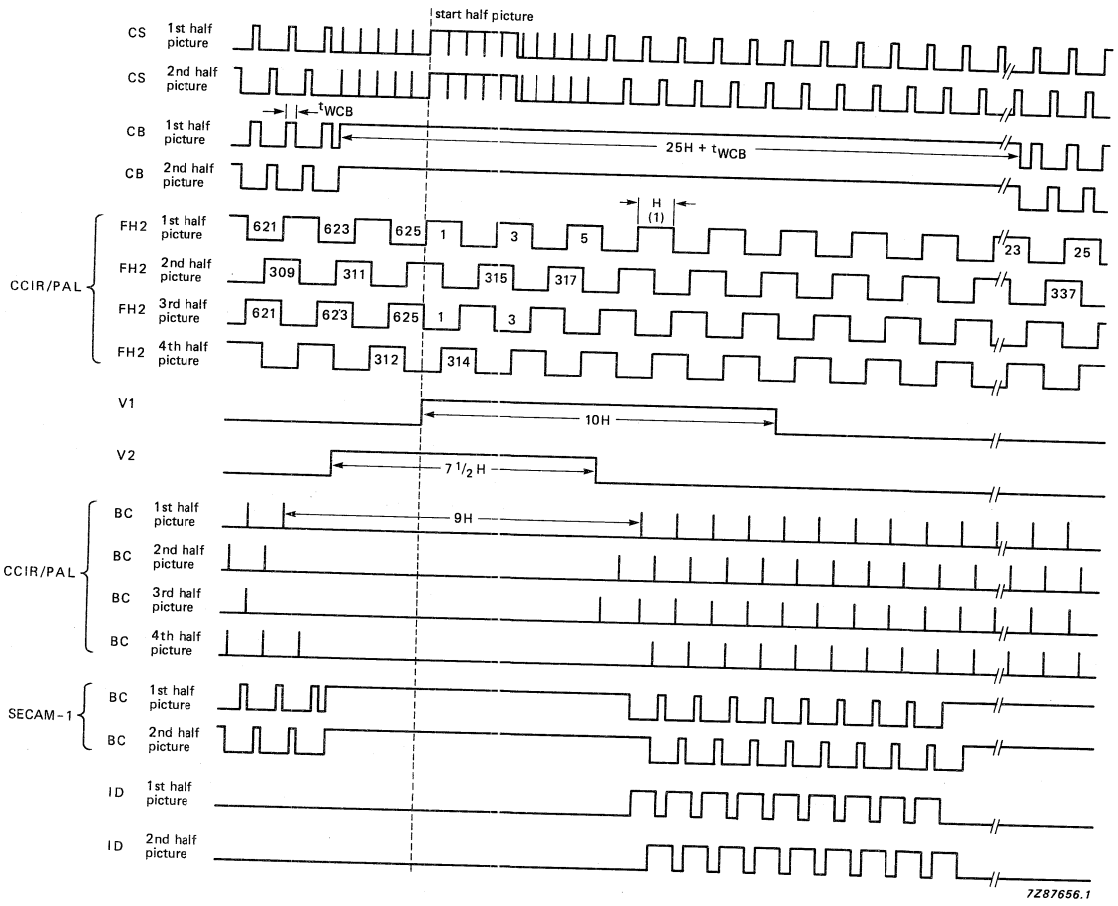
(3) Waveform at DL with two additional pulses decreases the number of horizontal scans per half picture by 1.

Fig. 6 Manipulation of the horizontal frequency for non-standard systems.

FUNCTIONAL DESCRIPTION (continued)

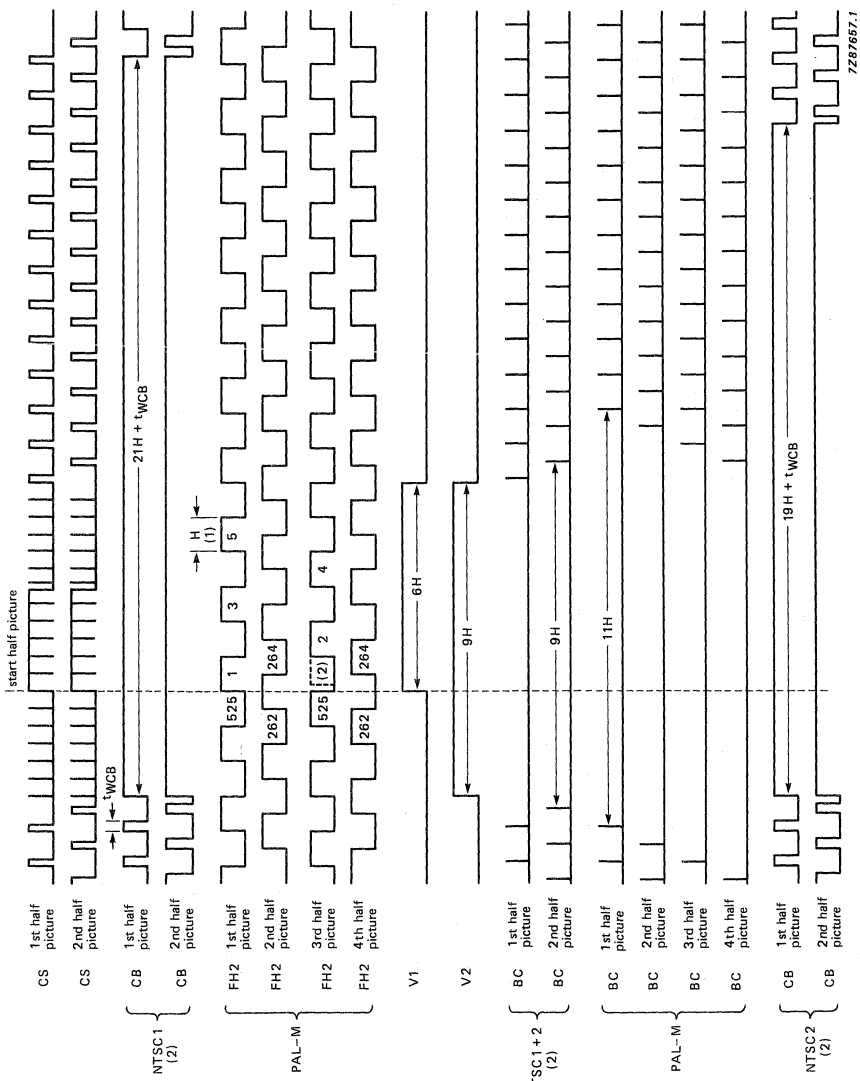
Output waveforms

The output waveforms for the different modes of operation are shown in Figs 7 and 8.



(1) H = 1 horizontal scan.

Fig. 7 Typical output waveforms for PAL/CCIR and SECAM. In the 624-line mode the output waveforms are identical to the 1st half picture of PAL/CCIR and are not interlaced (0.5 H subtracted from the waveform timing).



(1) H = 1 horizontal scan.
(2) NTSC mode reset; the 4th half picture is identical to the 2nd half picture for NTSC.

Fig. 8 Typical output waveforms for NTSC and PAL-M. In the 524-line mode the output waveforms are identical to the 1st half picture of NTSC and are not interlaced (0.5 H subtracted from the waveform timing).

WAVEFORM TIMING (Table 3, Figs 9 and 10)

The waveform timing depends on the frequency of the oscillator input (f_{OSCI}). This is shown in Table 3 as the number (n) of oscillations at OSCI. The timings given are derived from $n \times t_{OSCI} \pm 100$ ns. One horizontal scan (H) = $320 \times t_{OSCI} = 1/f_H$. Note that the number of horizontal scans per half picture can be modified for non-standard systems using input/output DL as shown in Fig. 6.

Table 3 Waveform timing

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
CS							
Horizontal sync pulse width	t_{WSC1}	4.8	4.77	4.77	4.8	µs	24
Equalizing pulse width	t_{WSC2}	2.4	2.38	2.38	2.4	µs	8
Serration pulse width	t_{WSC3}	4.8	4.77	4.77	4.8	µs	24
Duration of pre-equalizing pulses		2.5	3	3	2.5	H	
Duration of post-equalizing pulses		2.5	3	3	2.5	H	
Duration of serration pulses		2.5	3	3.5	2.5	H	
CB							
Horizontal blanking pulse width							
PAL/SECAM/PAL-M	t_{WCB}	12	–	11.12	12	µs	60
NTSC 1	t_{WCB}	–	11.12	–	–	µs	56
NTSC 2	t_{WCB}	–	10.53*	–	–	µs	53
Front porch	t_{PCBCS}	1.6	1.59	1.59	1.6	µs	8
Duration of vertical blanking							
PAL/SECAM/PAL-M		25H+t_{WCB}	–	21H+t_{WCB}	25H+t_{WCB}		
NTSC 1		–	21H+t_{WCB}	–	–		
NTSC 2		–	19H+t_{WCB}	–	–		
BC (PAL)							
Burst key pulse width	t_{WBC}	2.4	2.38	2.38	–	µs	12
Sync to burst delay	t_{PCSBC}	5.6	5.56	5.76	–	µs	28
Burst suppression		9	9	11	–	H	
Position of burst suppression: 1st half picture		H623 to H6	H523 to H6	H523 to H8	– –		
2nd half picture		H310 to H318	H261 to H269	H260 to H270	– –		
3rd half picture		H622 to H5	H523 to H6	H522 to H7	– –		
4th half picture		H311 to H319	H261 to H269	H259 to H269	– –		

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
BC (SECAM)							
Chrominance pulse width	t_{WBC}	–	–	–	7.2	µs	36
Chrominance to sync delay	t_{PBCCS}	–	–	–	1.6	µs	8
Duration of vertical blanking: SECAM 1	1st half picture : 25H + t_{WBC} except H320 to H328 2nd half picture: 24.5H + t_{WBC} except H7 to H15						
SECAM 2	1st half picture : 25H + t_{WBC} 2nd half picture: 24.5H + t_{WBC}						
CLP							
Clamp pulse width	t_{WCLP}	2.4	2.38	2.38	2.4	µs	12
Sync to clamp delay	t_{PCSCLP}	2.4	2.38	2.38	2.4	µs	12
DL							
Frequency	f_{DL}	2 x f_H	2 x f_H	2 x f_H	2 x f_H		
Pulse width	t_{WDL}	9.6	9.53	9.53	9.6	µs	48
DL to sync delay	t_{PCLCS}	5.6	5.56	5.56	5.6	µs	28
FH80							
Frequency	f_{FH80}	80 x f_H	80 x f_H	80 x f_H	80 x f_H		
Sync to FH80 delay		0.2	0.2	0.2	0.2	µs	1
H1, H2							
H1 pulse width	t_{WH1}	7.2	7.15	7.15	7.2	µs	36
H2 pulse width	t_{WH2}	7.2	7.15	7.15	7.2	µs	36
H1 to sync delay	t_{PH1CS}	0.8	0.79	0.79	0.8	µs	4
Sync to H2 delay	t_{PCSH2}	0.8	0.79	0.79	0.8	µs	4
Repetition period		64	63.56	63.56	64	µs	
V1, V2							
V1 duration		10	6	6	10	H	
V2 duration		7.5	9	9	7.5	H	
V1 to sync delay	t_{PV1CS}	1.6	1.59	1.59	1.6	µs	8
Sync to V2 delay	t_{PV2CS}	1.6	1.59	1.59	1.6	µs	8
FH2							
Frequency	f_{FH2}	$f_H/2$	$f_H/2$	$f_H/2$	$f_H/2$		
Sync to FH2 delay		0	0	0	0	µs	
FH3							
Frequency	f_{FH3}	400	360	360	$f_H/3$		
Sync to FH3 delay		–	–	–	0	µs	

WAVEFORM TIMING (continued)

Table 3 (continued)

parameter	symbol	PAL	NTSC	PAL-M	SECAM	unit	n
WMP							
WMP pulse width		2.4	2.38	2.38	2.4	μs	12
Sync to WMP delay		34.4	34.16	34.16	34.4	μs	172
Duration of WMP		10	9	9	10	H	
Position of WMP							
1st half picture:		H163 to H173	H134 to H143	H134 to H143	H163 to H173		
2nd half picture:		H475 to H485	H396 to H405	H396 to H405	H475 to H485		
RI							
Frequency		$f_V/2$	$f_V/2$	$f_V/2$	$10f_H$		
Position of edges		H6 and H318	H7 and H269	H7 and H269	—		
ID							
ID pulse width	t_{WID}	12.0	11.12	11.12	12.0	μs	60
ID to sync delay	t_{PIDCS}	1.6	1.59	1.59	1.6	μs	8
Position of ID							
1st half picture:		H7 to H15	H8 to H22	H8 to H22	H7 to H15		
2nd half picture:		H320 to H328	H271 to H285	H271 to H285	H320 to H328		

* Horizontal blanking pulse width for NTSC 2 can be 11.12 μs maximum.

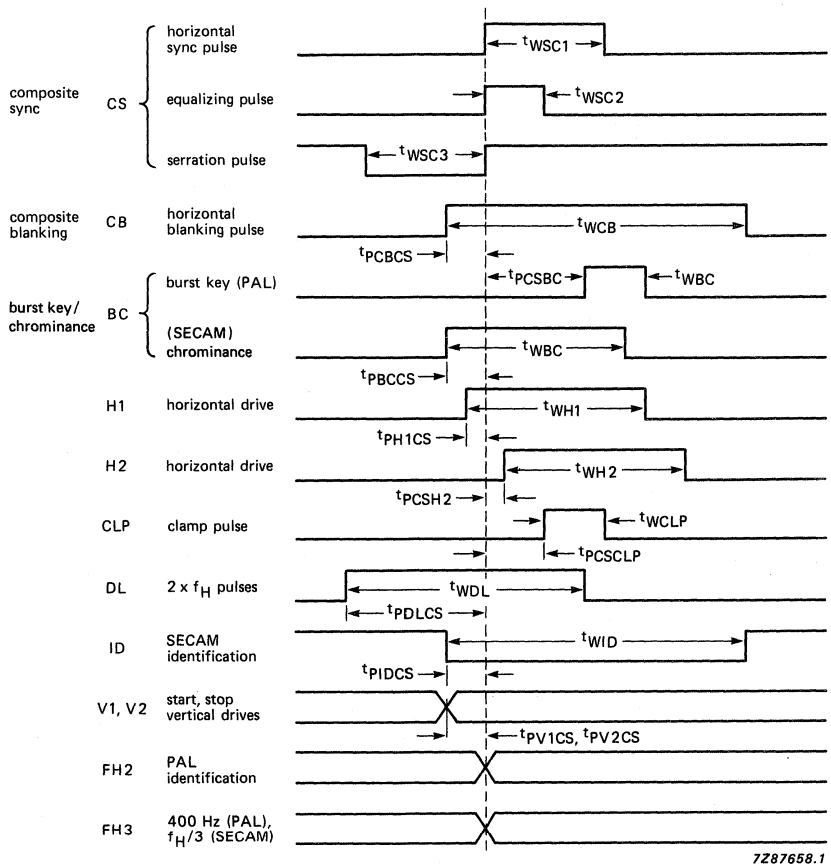


Fig. 9 Waveform timings; PAL/CCIR; SECAM; 624-line modes.

WAVEFORM TIMING (continued)

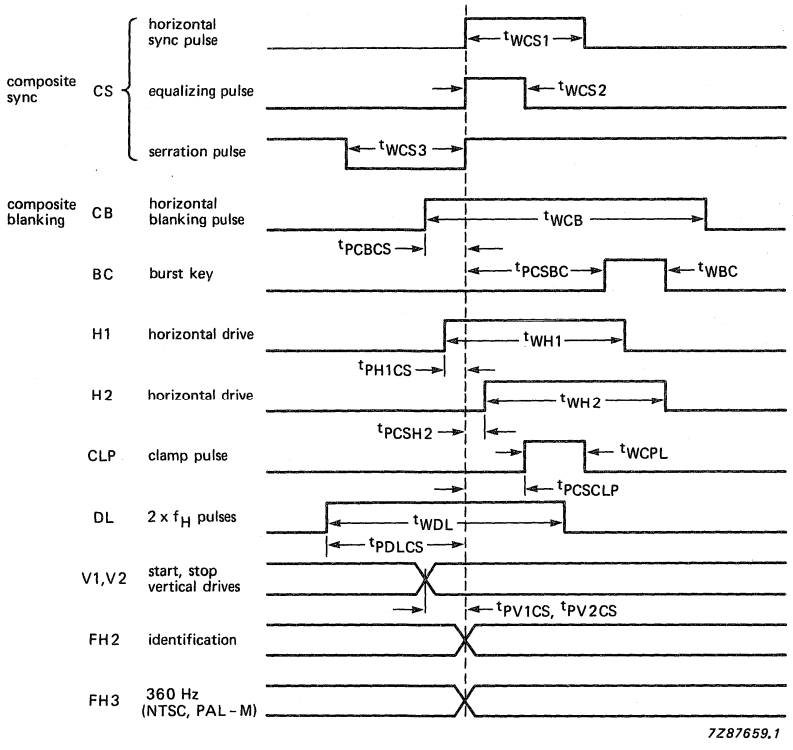


Fig. 10 Waveform timings: NTSC; PAL-M; 524-line modes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range with respect to V_{SS}	V_{DD}	−0.5	+ 15	V
Input voltage range	V_I	−0.5	V_{DD} + 0.5*	V
Input current	$\pm I_I$	–	10	mA
Output voltage range	V_O	−0.5	V_{DD} + 0.5*	V
Output current	$\pm I_O$	–	10	mA
Total power dissipation per package	P_{tot}	–	200	mW
Power dissipation per output	P_O	–	100	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* V_{DD} + 0.5 V not to exceed 15 V.

CHARACTERISTICS

V_{DD} = 5.7 to 7.5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5.7	–	7.5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current at V_I = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LI}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	$-I_{LI}$	–	–	1	μA
Outputs (except PH and OSC0)					
Output voltage HIGH at $-I_{OH}$ = 0.5 mA	V_{OH}	$V_{DD} - 0.5$	–	–	V
Output voltage LOW at I_{OL} = 0.5 mA	V_{OL}	–	–	0.4	V
Output PH					
Output voltage HIGH at $-I_{OH}$ = 0.9 mA	V_{OH}	$V_{DD} - 0.5$	–	–	V
Output voltage LOW at I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V	I_{LO}	–	–	5	μA
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LO}	–	–	1	μA
Output leakage current at V_O = 0 V; V_{DD} = 7.5 V	$-I_{LO}$	–	–	5	μA
Output leakage current at V_O = 0 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	$-I_{LO}$	–	–	1	μA
Output OSCO					
Output voltage HIGH at V_{OSCI} = 0 V; $-I_{OH}$ = 0.9 mA	V_{OH}	$V_{DD} - 0.5$	–	–	V
Output voltage LOW at V_{OSCI} = V_{DD}; I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V

parameter	symbol	min.	typ.	max.	unit
Input/output DL (open drain)*					
Output voltage LOW at I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V	I_{LO}	–	–	5	μA
Output leakage current at V_O = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LO}	–	–	1	μA
Load resistance (Fig. 4)					
at V_{DD} = 5.7 V	R_L	1.4	–	–	kΩ
at V_{DD} = 7.5 V	R_L	0.82	–	–	kΩ
Time constant (Fig. 4)					
at V_{DD} = 5.7 V	R_LC_L	–	–	19	ns
at V_{DD} = 7.5 V	R_LC_L	–	–	13	ns
Oscillator frequency (Fig. 4)					
Maximum oscillator frequency at V_{DD} = 5.7 V	f_{OSC}	5.1	–	–	MHz

* An external pull-up resistor (3.9 kΩ) must be connected between DL and V_{DD}. The time constant R_LC_L must not exceed the values given.

APPLICATION INFORMATION

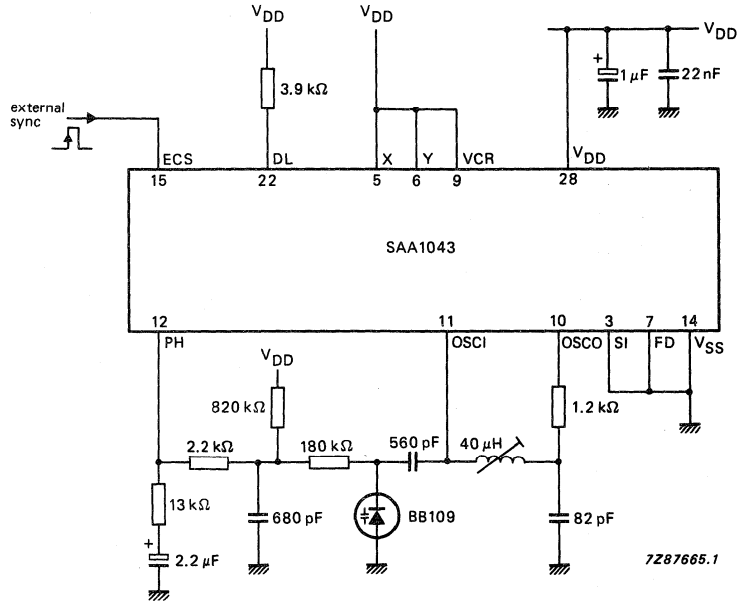


Fig. 11 Synchronizing circuit using passive filter network.

SUBCARRIER COUPLER

GENERAL DESCRIPTION

The SAA1044 maintains the correct relationship between subcarrier and horizontal scan frequencies when an exact coupling is required. It is for use in combination with sync generator SAA1043 for application in colour video sources (cameras, film-scanners and similar equipments).

Features

- Provides exact relationship between subcarrier and horizontal scan frequencies
- Accommodates all standard frequencies
- Facilitates GENLOCK (general locking) applications

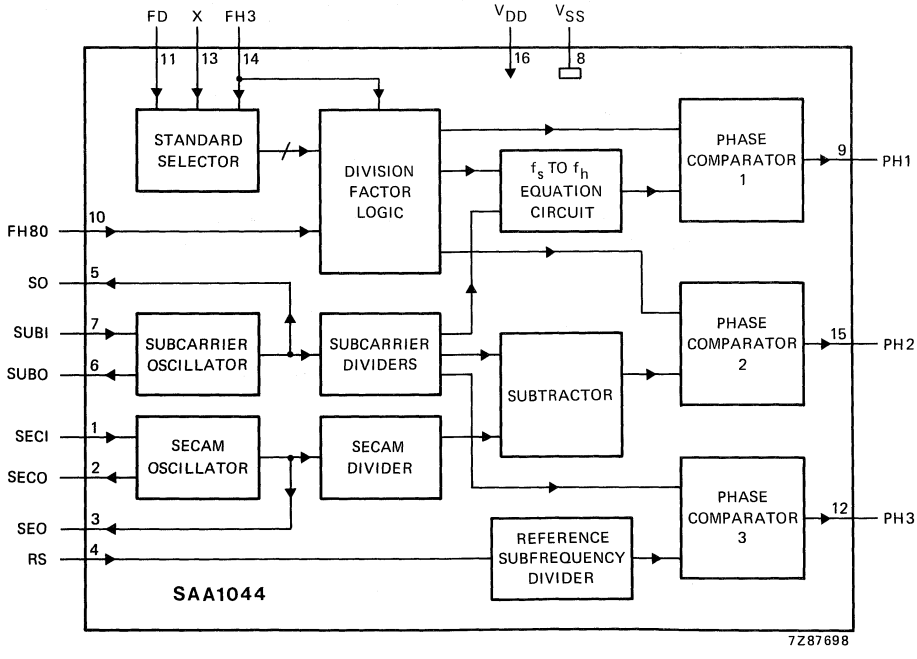


Fig.1 Block diagram.

PACKAGE OUTLINES

SAA1044: 16-lead DIL; plastic (SOT38).
SAA1044T: 16-lead mini-pack; plastic (SO16L; SOT162A).

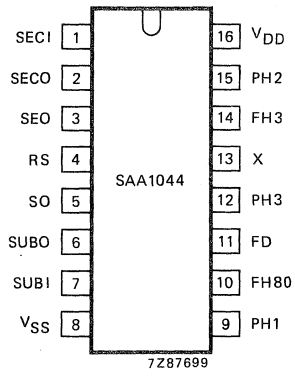


Fig. 2 Pinning diagram.

PINNING

1	SECI	SECAM oscillator input ($272f_H$)
2	SECO	SECAM oscillator output ($272f_H$)
3	SEO	inverted SECAM oscillator output
4	RS	reference subfrequency
5	SO	inverted subcarrier oscillator output
6	SUBO	subcarrier oscillator output
7	SUBI	subcarrier oscillator input
8	V_{SS}	negative supply voltage (ground)
9	PH1	phase comparator 1 output (FH80/SUBI)
10	FH80	1.25 MHz input (from SAA1043)
11	FD	standard programming input
12	PH3	phase comparator 3 output (RS/SUBI)
13	X	standard programming input
14	FH3	standard programming input (from SAA1043)
15	PH2	phase comparator 2 output (SECI/FH80)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

Programming of operating standard

The standard required for operation is programmed using the inputs FD, X and FH3 as shown in Table 1.

Table 1 Programming of operating standard

standard	FD	X	FH3	relationship of subcarrier frequency (f_S) to horizontal scan frequency (f_H)
PAL	0	1	400 Hz	$f_S = 283.7516f_H$
SECAM	0	0	don't care	$f_S = 282f_H$
PAL-N	1	1	400 Hz	$f_S = 229.2516f_H$
PAL-M	1	0	1	$f_S = 227.25f_H$
NTSC	1	0	0	$f_S = 227.5f_H$

Positive logic: 1 = HIGH; 0 = LOW

Subcarrier/horizontal scan frequency relationship

The input FH80 from SAA1043 is the reference for horizontal scan frequency (f_H). This frequency is reduced by a factor determined by the selected operating standard to give a value of $8f_H$ (PAL, SECAM) or $10f_H$ (PAL-N, PAL-M, NTSC) to phase comparator 1. The subcarrier frequency (f_S) is manipulated to provide a comparable value at the second input to the phase comparator. When the frequencies of the two inputs to phase comparator 1 are equal, the relationship between f_H and f_S is as shown in Table 1.

Phase comparator 1 functions with an exclusive-OR phase detector circuit and provides an output which may be used to control a voltage-controlled oscillator (VCO) via a low-pass filter. The VCO reference can be the subcarrier or the horizontal scan frequency and the filter can be active or passive, depending on application.

A second subcarrier oscillator circuit is provided for SECAM operation. The operating frequency of this is centred on $272f_H$ to give, when $f_S = 282f_H$, comparable values of $5f_H$ at the two inputs to phase comparator 2. A second VCO loop can be used to control the SECAM oscillator frequency.

The high degrees of accuracy and stability required for GENLOCK applications are met by phase comparator 3. This compares the internal subcarrier and external reference frequencies. To adjust the phase over 2π, this comparator has a linear characteristic over 4π. The output signal PH3 has a period time of $f_S/4$ and a duty factor of between 12.5% and 62.5% giving a sensitivity of 240 mV/rad. Errors due to temperature variation are minimized by symmetrical circuit and chip design.

RATINGS

parameter	symbol	min.	max.	unit
Supply voltage range with respect to V_{SS}	V_{DD}	−0.5	+ 15	V
Input voltage range	V_I	−0.5	V_{DD} + 0.5*	V
Input current	$\pm I_I$	−	10	mA
Output voltage range	V_O	−0.5	V_{DD} + 0.5*	V
Output current	$\pm I_O$	−	10	mA
Total power dissipation per package	P_{tot}	−	200	mW
Power dissipation per output	P_O	−	100	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

HANDLING

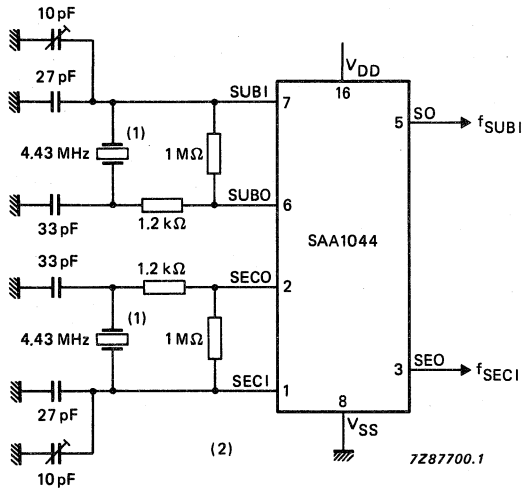
Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

* V_{DD} + 0.5 V not to exceed 15 V.

CHARACTERISTICS

V_{DD} = 5.7 to 7.5 V; V_{SS} = 0 V; T_{amb} = −25 to + 70 °C unless otherwise specified

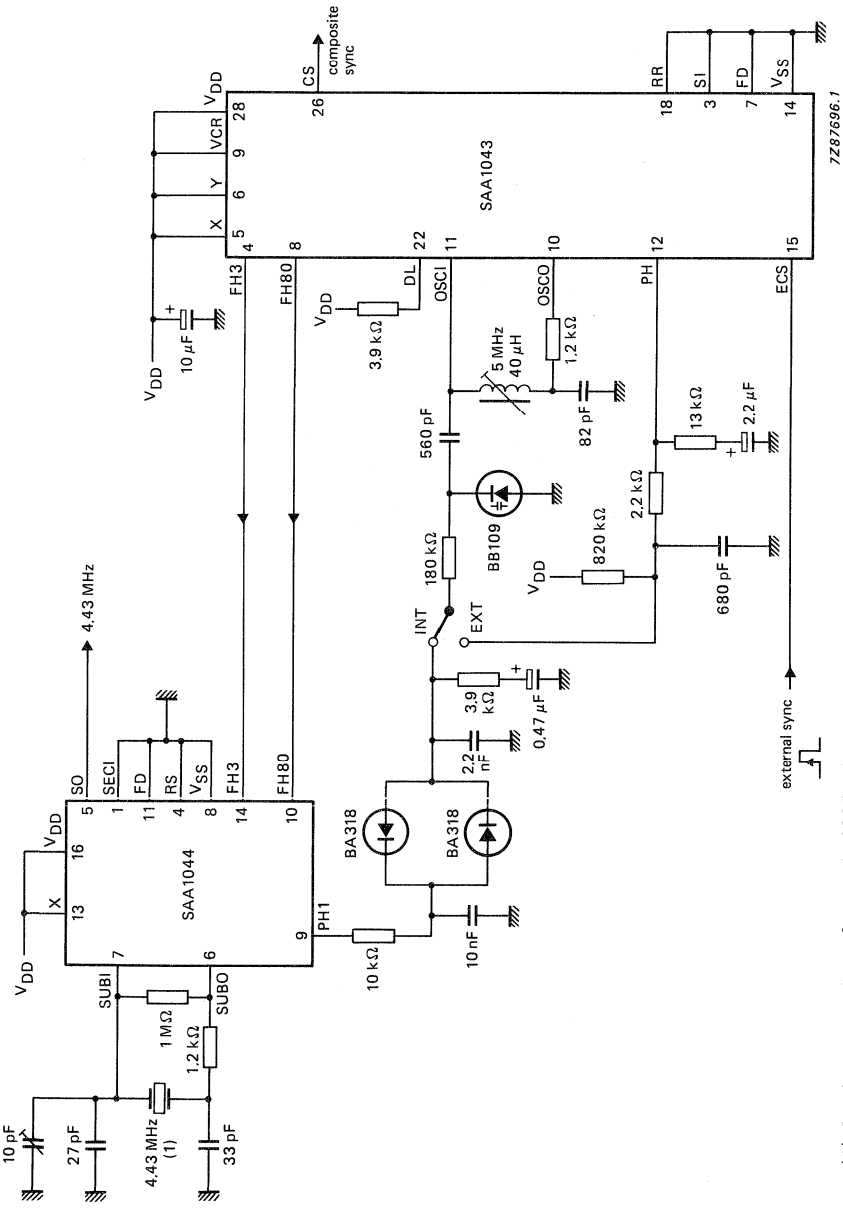
parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage	V_{DD}	5.7	–	7.5	V
Supply current (quiescent) at I_O = 0 mA at all outputs; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{DD}	–	–	10	μA
Inputs					
Input voltage HIGH	V_{IH}	$0.7V_{DD}$	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	$0.3V_{DD}$	V
Input leakage current at V_I = 7.5 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	I_{LI}	–	–	1	μA
Input leakage current at V_I = 0 V; V_{DD} = 7.5 V; T_{amb} = 25 °C	$-I_{LI}$	–	–	1	μA
Outputs (except SECO and SUBO)					
Output voltage HIGH at $-I_{OH}$ = 0.5 mA	V_{OH}	V_{DD} −0.5	–	–	V
Output voltage LOW at I_{OL} = 0.5 mA	V_{OL}	–	–	0.4	V
Outputs SECO and SUBO					
Output voltage HIGH at $-I_{OH}$ = 0.9 mA	V_{OH}	V_{DD} −0.5	–	–	V
Output voltage LOW at I_{OL} = 1.0 mA	V_{OL}	–	–	0.4	V
Oscillator frequency (Fig.3)					
Maximum oscillator frequency at V_{DD} = 5.7 V					
pin 1	f_{SECI}	5.1	–	–	MHz
pin 7	f_{SUBI}	5.1	–	–	MHz



(1) Catalogue number of crystal: 4322 143 04040.
(2) Inputs not shown are don't care.

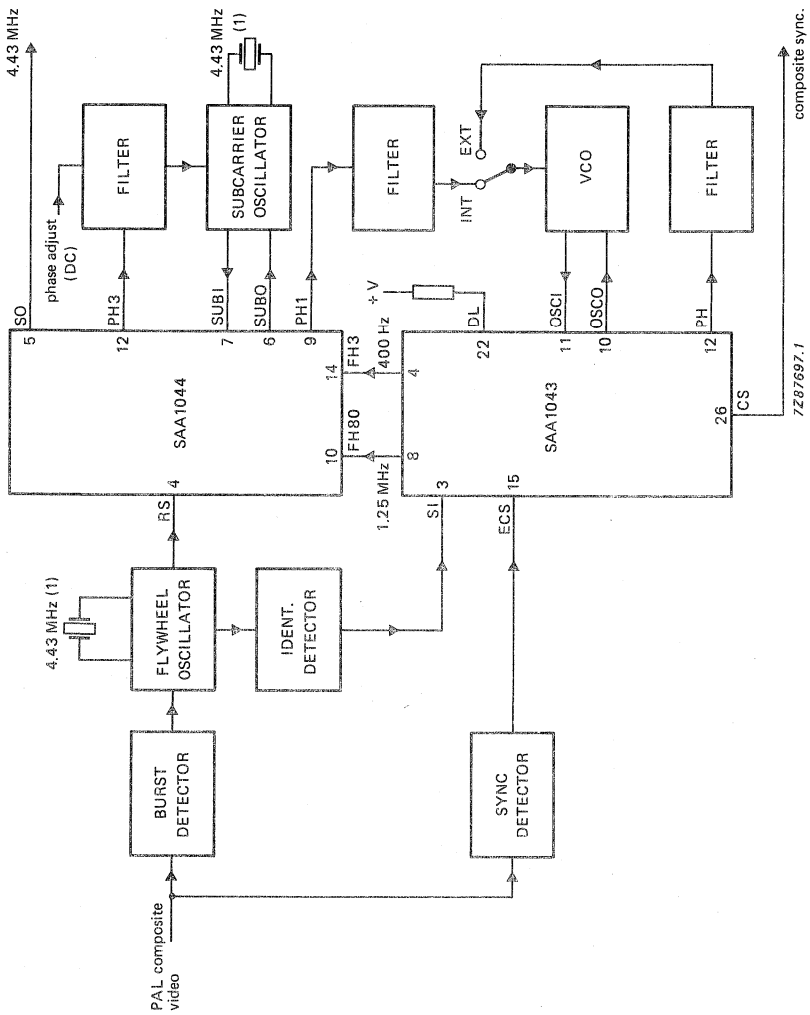
Fig.3 Test set-up for oscillator frequency measurement.

APPLICATION INFORMATION



(1) Catalogue number of crystal: 4322 143 04040.

Fig.4 Subcarrier coupling for PAL application; external synchronization is selected with switch in EXT condition.



(1) Catalogue number of crystal: 4322 143 04040.

Fig.5 Subcarrier coupling for PAL GENLOCK application.

MULTI-NORM PULSE-PATTERN GENERATOR

GENERAL DESCRIPTION

The SAD1019 is part of a frame transfer image sensor camera system which uses the NXA series of frame transfer image sensors. The device provides the vertical transport pulses necessary, for the operation of the frame transfer image sensors and a start-stop signal for the horizontal clock generator. The drive pulses and clock signals for the SAD1019 are provided by the universal sync generator (SAA1043).

Features

- Vertical transport pulses for the image region and storage region of the image sensor during field blanking (ϕ_A and ϕ_B pulses)
- Colour separation and transport of one line of sensor information to the output register during line blanking (ϕ_B, TG and ϕ_C pulses)
- Other additional pulses required for the control and processing in the frame transfer image sensor camera

PACKAGE OUTLINES

SAD1019: 24-lead DIL; plastic (SOT101B).
SAD1019T: 24-lead mini-pack; plastic (SO24; SOT137A).

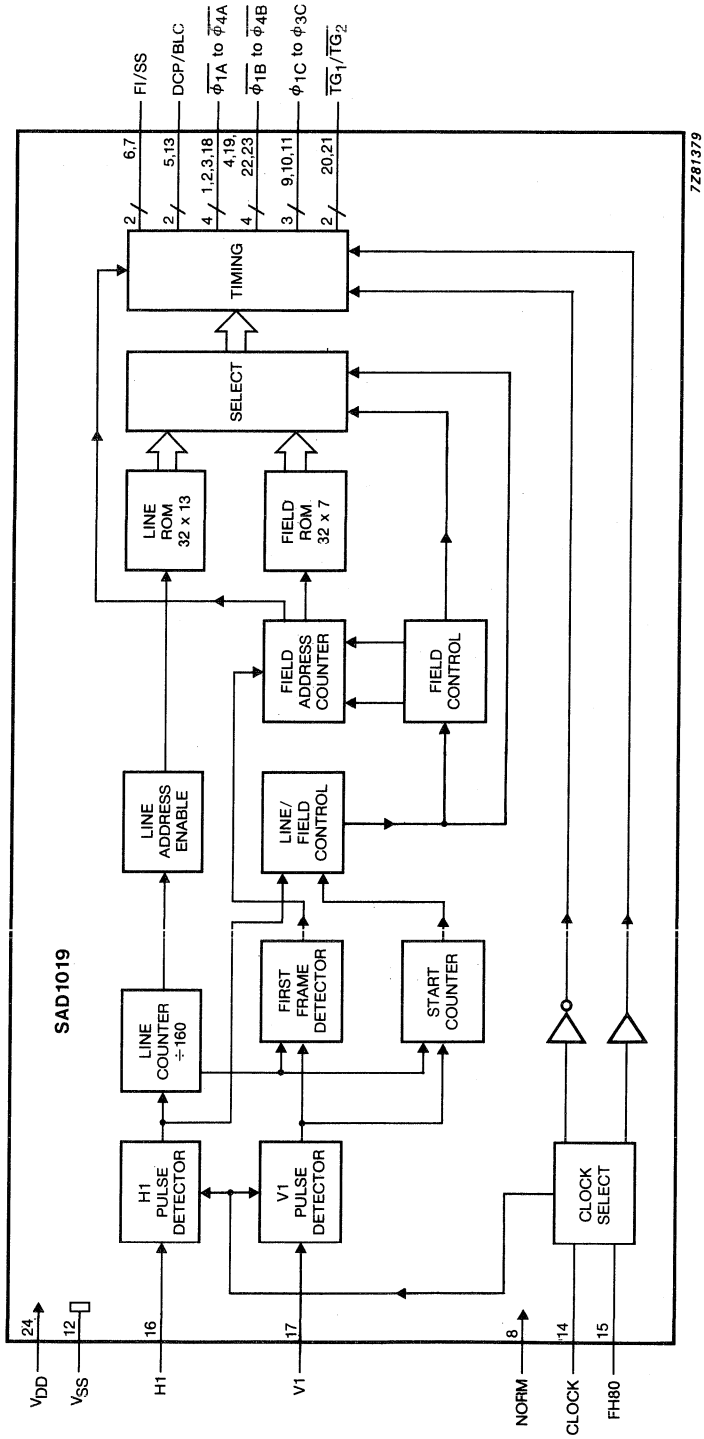


Fig.1 Block diagram.

PINNING

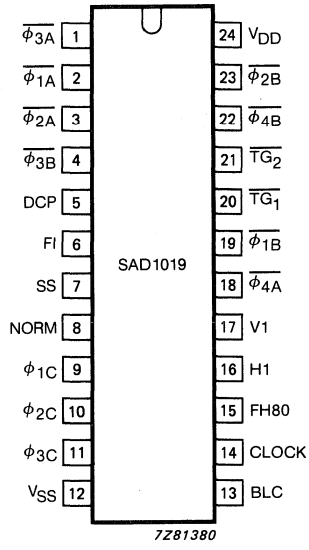


Fig.2 Pinning diagram.

DEVELOPMENT DATA

Power supplies

V_{DD}	positive supply voltage (+ 5 V)
V_{SS}	ground (0 V)

Inputs (CMOS)

CLOCK	clock input from SAA1043, typ. 2.5 MHz (625 lines) or typ. 2.51748 MHz (525 lines). 5 MHz mode, typ. 5 MHz (625 lines) or 5.03496 MHz (525 lines)
FH80	clock input from SAA1043, typ. 1.25 MHz (625 lines) or 1.25874 MHz (525 lines)
H1	H1 input from SAA1043, typ. 15.625 kHz (625 lines) or typ. 15.734 kHz (525 lines)
V1	V1 input from SAA1043, typ. 50 Hz (625 lines) or 59.94 Hz (525 lines)
NORM	norm-selection input, 625 lines = LOW, 525 lines = HIGH

Outputs (CMOS push-pull)

$\overline{\phi 1A}$ to $\overline{\phi 4A}$	sensor image section control to drivers
$\overline{\phi 1B}$ to $\overline{\phi 4B}$	sensor storage section control to drivers
$\phi 1C$ to $\phi 3C$	low frequency outputs for transport pulses to pixel oscillator
DCP	DC clamp pulse
FI	frame identification
SS	start/stop for pixel generator
BLC	black-level clamping
$\overline{TG1}$ and $\overline{TG2}$	transfer gate control to drivers

FUNCTIONAL DESCRIPTION

625 line mode (NORM = LOW, see Figs 3 to 7)

One complete cycle of the multi-norm pulse-pattern generator (MNPPG) occurs after a command from the synchronization pulse generator (SYN). This cycle consists of 294 line cycles which are used to read out the sensor information followed by transport of the integrated information from the image area to the storage area of the sensor. Once this cycle has been completed the device enters into a 'wait' status period which lasts until the device receives a start command from the SYN.

The cycle is restarted with a V-pulse from the SYN. The falling edge of this pulse is detected in the MNPGG and results in a reset of the start counter as well as providing the field information (field 1/2). The start counter counts 11 lines and then the line cycle information is read from the line ROM. The start of the line cycle occurs at line 22 in frame 1 and line 335 in frame 2. The H1 pulse of the SYN controls the position of the line cycle with respect to the SYN pulses. The H1 pulse sets the correct value in the line counter of the MNPPG.

The control counter counts the number of line cycles and switches the line cycle to field cycle after 294 lines (in both fields), then the field cycle information is read from the field ROM. The control counter was reset before the switch over had taken place, it now counts the field cycles. The field cycle lasts for 294 cycles of the $\overline{\phi 4B}$ pulse and then the device enters the wait status period again.

The device will continue to operate in the manner described, until the overall system is switched off.

525 line mode (NORM = HIGH)

The basic operation is identical except for variations in the start points and number of transports (see Figs 8 to 12).

Operating modes

Synchronization generator (SAA1043)

The H1 pulse from the SAA1043, due to internal delays, is out of phase with the MNPPG clock signal. The following method is used to obtain the correct phase relationship between the H1 pulse and the MNPPG output. The H1 pulse and the FH80 are clocked into a flip-flop, at the output of the flip-flop the timing of the H1 and FH80 signals are in phase. The output of the flip-flop is sampled with that of the CLOCK, which is in phase with the FH80. In this way a reliable fixed phase relationship between SYN and MNPPG is obtained.

Other operating modes

- single 2.5 MHz operation:
  If another synchronization pulse generator is used, in which an H1 pulse is in phase with the CLOCK, a single 2.5 MHz clock signal can be used.

  Connect the 2.5 MHz to the CLOCK and with delay circuitry (RC elements, 50 ns approx.) to FH80.
- single 5 MHz operation:
  If another synchronization pulse generator is used, in which an H1 pulse is in phase with the CLOCK, a single 5 MHz clock signal can be used.

  Connect the 5 MHz to the CLOCK and connect FH80 to ground.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range (pin 24)	V_{DD}	−0.5	+ 7.0	V
Supply current (pin 24)	I_{DD}	−	50	mA
Supply current (pin 12)	I_{SS}	−	50	mA
Input voltage range	V_I	−0.5	V_{DD} + 0.5*	V
Input current	$\pm I_I$	−	10	mA
Output current	$\pm I_O$	−	10	mA
Total power dissipation per package	P_{tot}	−	500	mW
Power dissipation per output	P_O	−	25	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−55	+ 150	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is good practice to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

DEVELOPMENT DATA

* V_{DD} + 0.5 V not to exceed 7.0 V.

CHARACTERISTICS

V_{DD} = 4.5 to 5.5 V; T_{amb} = 25 °C, unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Current						
Supply current	on all outputs; I_O = 0 mA	I_{DD}	–	–	10	μA
Inputs H1, V1, NORM, CLOCK and FH80						
Input voltage HIGH		V_{IH}	$0.7V_{DD}$	–	–	V
Input voltage LOW	CMOS compatible	V_{IL}	–	–	$0.3V_{DD}$	V
Outputs						
Output voltage HIGH	all outputs except BLC; $-I_O$ = 0.8 mA; V_{DD} = 5 V	V_{OH}	–	–	$V_{DD}-0.5$	V
Output voltage LOW	all outputs except BLC; I_O = 2.9 mA; V_{DD} = 5 V	V_{OL}	–	–	0.5	V
Black level clamping (BLC)						
Output voltage HIGH	$-I_O$ = 2.6 mA; V_{DD} = 5 V	V_{OH}	–	–	$V_{DD}-0.5$	V
Output voltage LOW	I_O = 2.9 mA; V_{DD} = 5 V	V_{OL}	–	–	0.5	V

DEVELOPMENT DATA

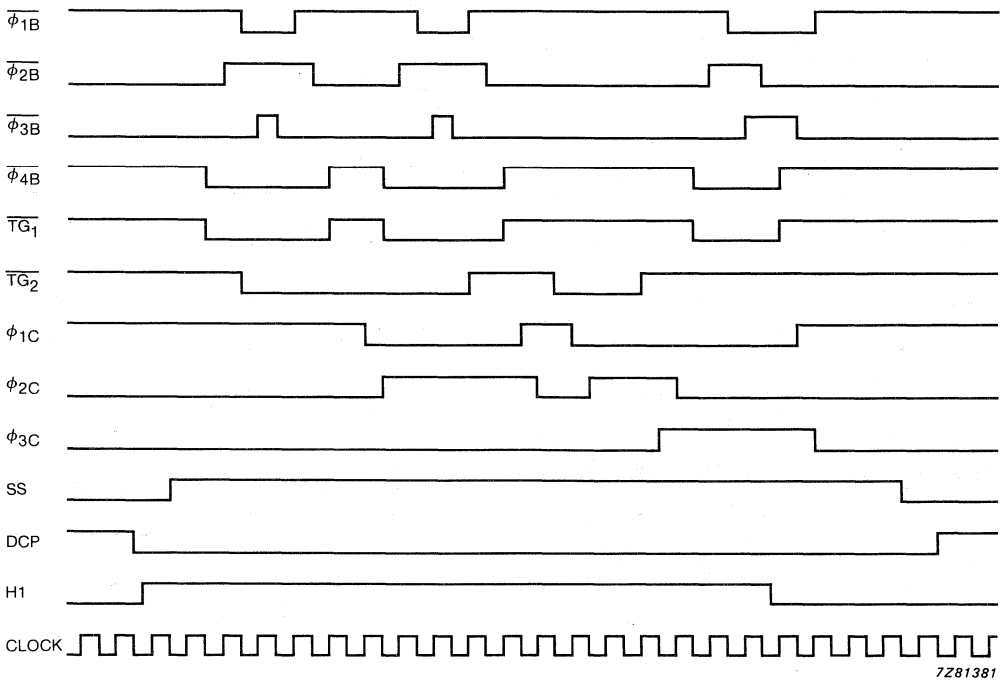
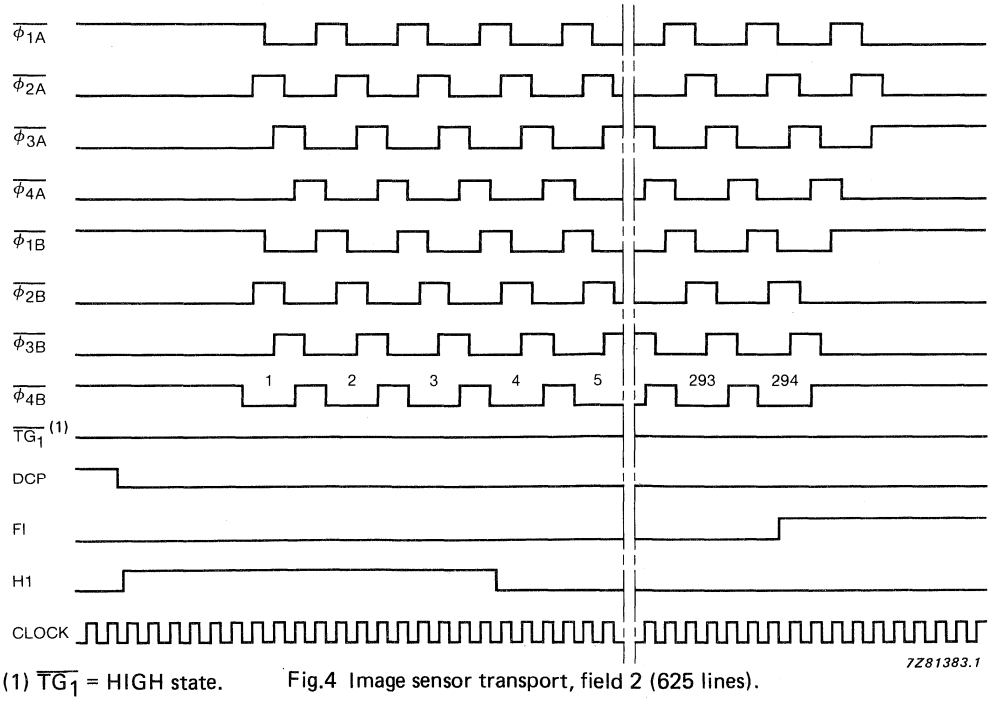
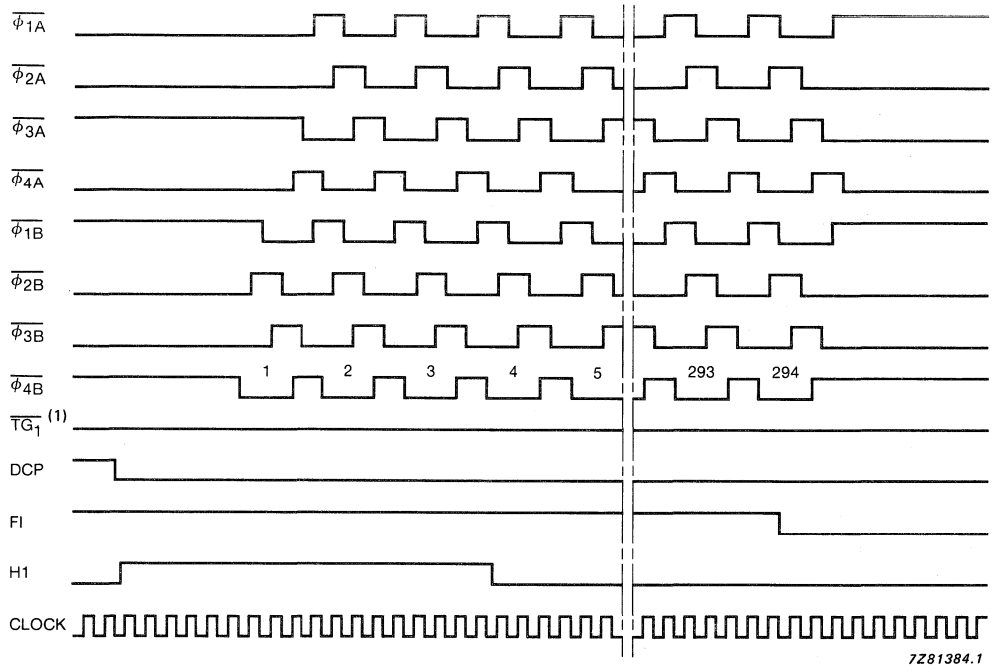


Fig.3 Line transport (625 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.4 Image sensor transport, field 2 (625 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.5 Image sensor transport, field 1 (625 lines).

DEVELOPMENT DATA

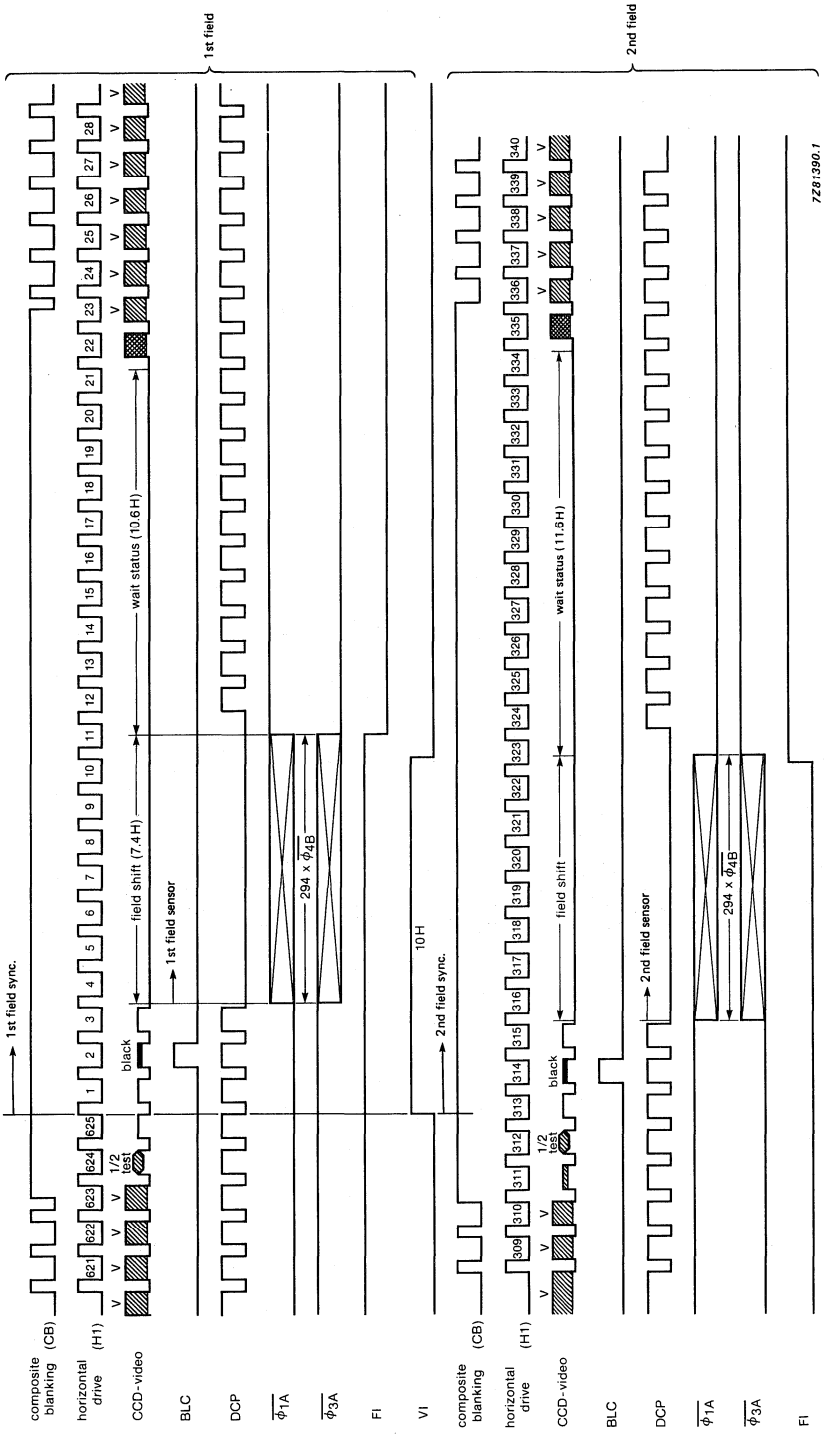


Fig.6 Pulse pattern during field blanking (625 lines).

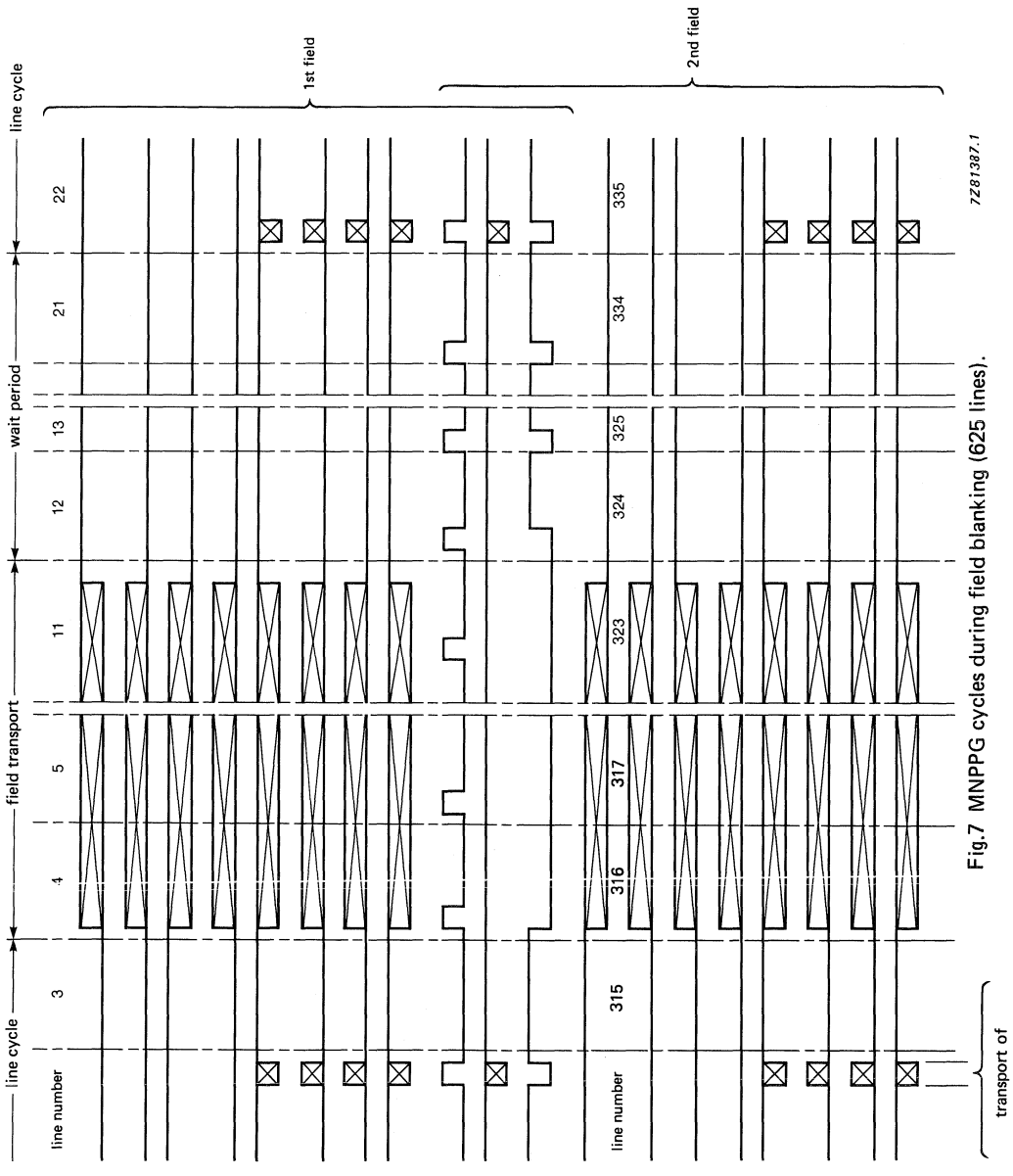


Fig.7 MNPPG cycles during field blanking (625 lines).

DEVELOPMENT DATA

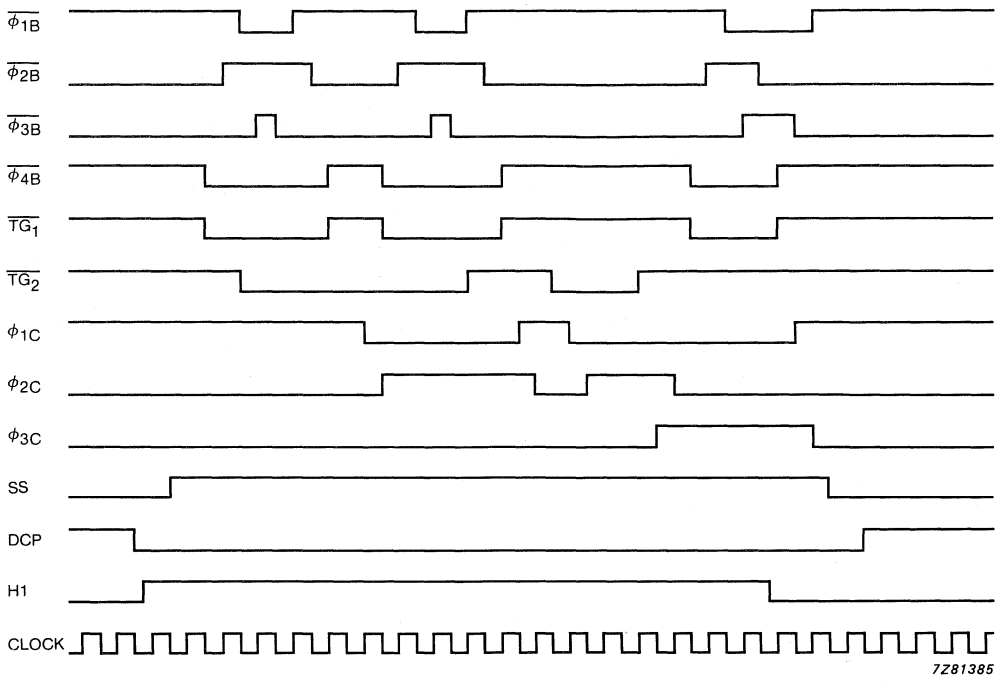
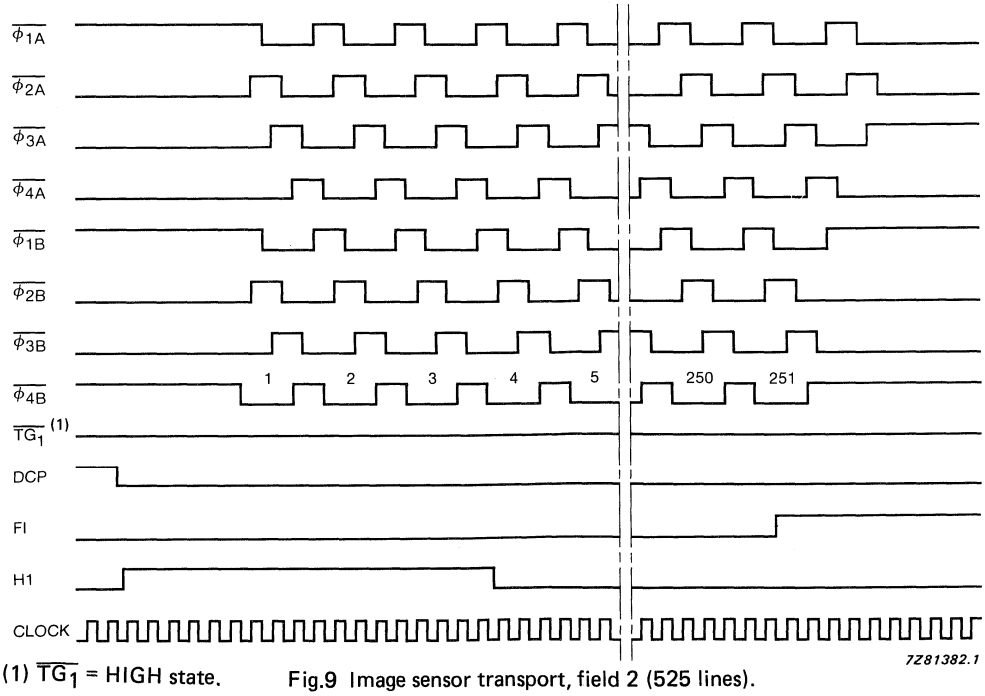
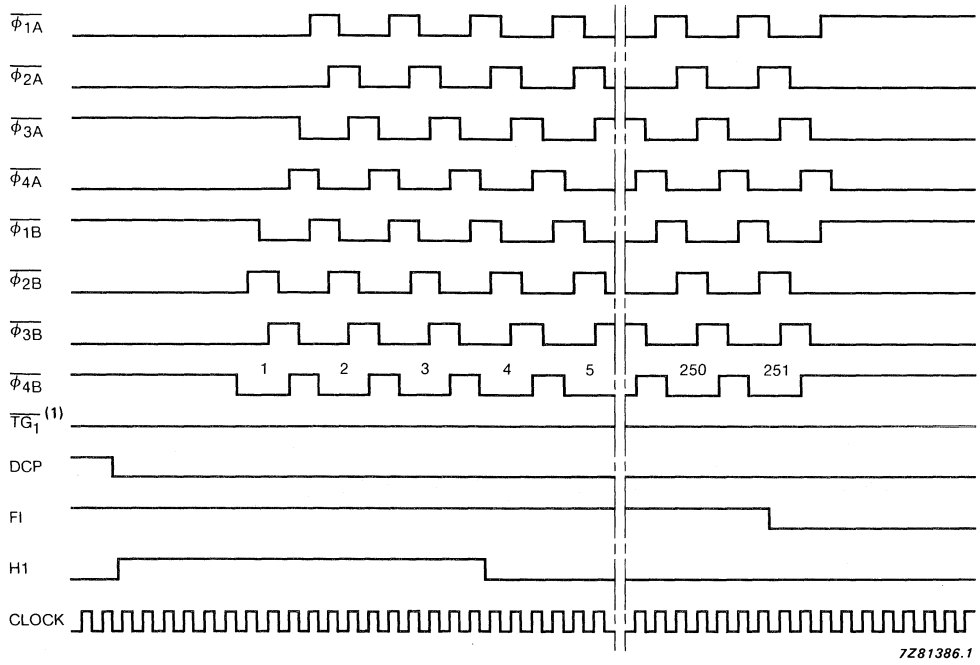


Fig.8 Line transport (525 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.9 Image sensor transport, field 2 (525 lines).



(1) $\overline{TG_1}$ = HIGH state.

Fig.10 Image sensor transport, field 1 (525 lines).

DEVELOPMENT DATA

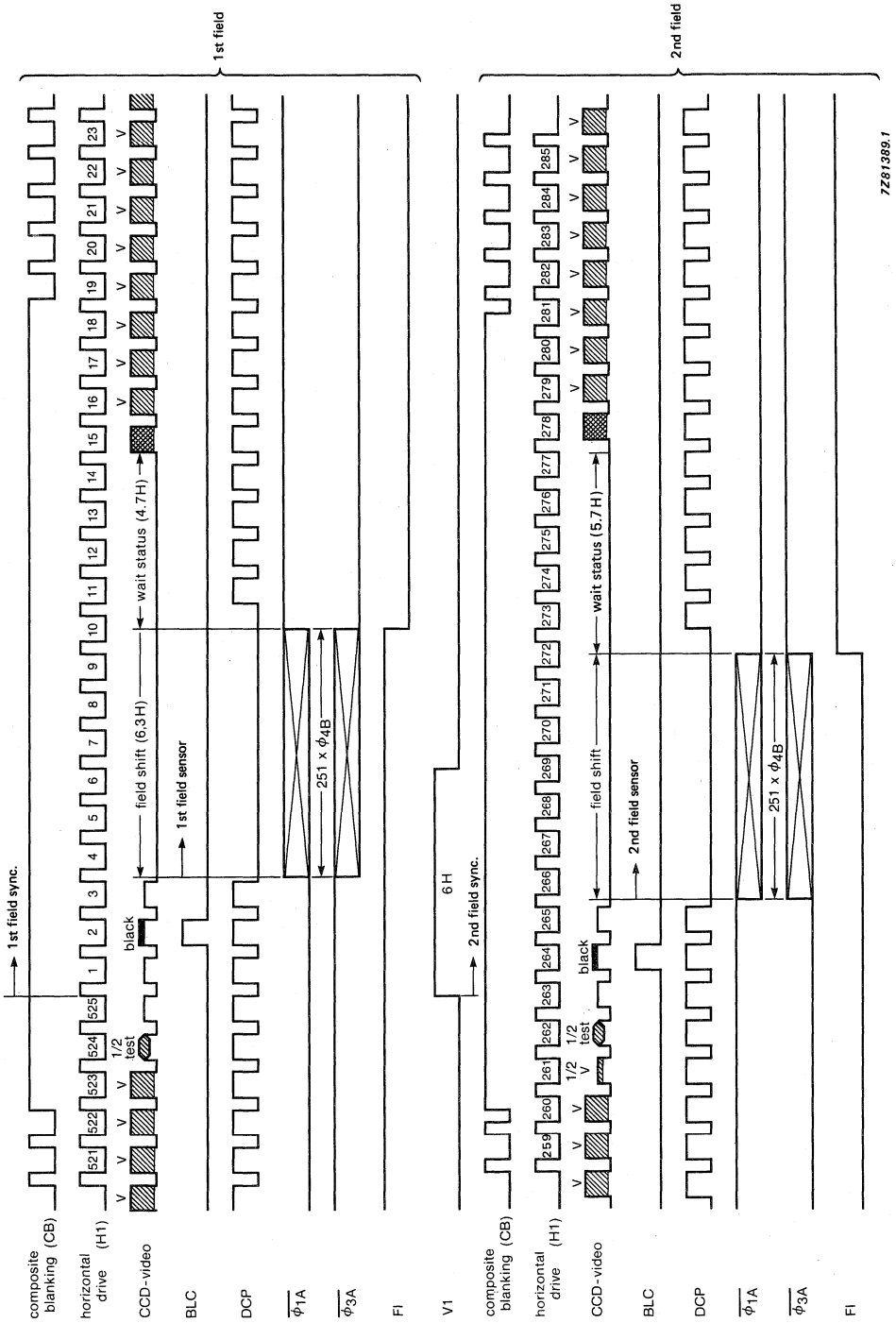


Fig.11 Pulse pattern during field blanking (525 lines

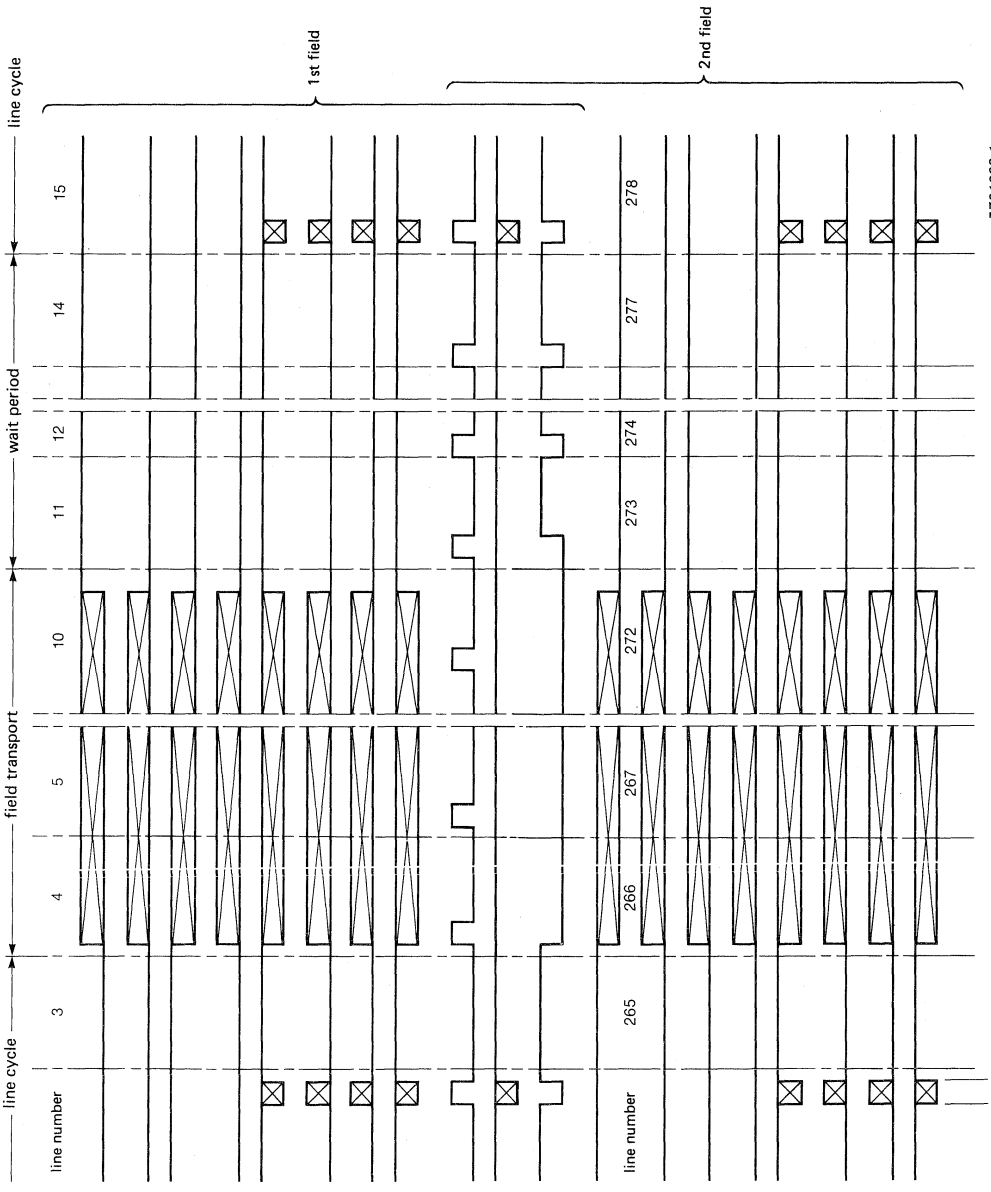


Fig.12 MNPPG cycles during field blanking (525 lines).

VERTICAL DRIVER

GENERAL DESCRIPTION

The TDA4301 is an integrated circuit which acts as an inverting buffer between the pulse pattern generator SAD1019 (LOCMOS technology) and the NXA1011 to NXA1041 frame-transfer sensors. The circuit consists of four drivers either for all vertical transfer clocks for image part (1A to 4A), or all vertical transfer clocks for storage part (1B to 4B) electrodes, and one driver for a transfer gate (TG) electrode.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltages						
pin 13		$V_{13\text{-}16}$	4.5	5.0	5.5	V
pin 1		$V_{1\text{-}16}$	11.0	11.25	11.5	V
Supply current	$V_{13\text{-}16}$ = 5 V	I_{13}	–	14	–	mA
Operating current	$V_{1\text{-}16}$ = 11.25 V	I_1	–	9.25	–	mA
Storage temperature range		T_{stg}	−25	–	+150	°C
Operating ambient temperature range		T_{amb}	−20	–	+70	°C

PACKAGE OUTLINE

16-lead DIL; plastic (SOT38).

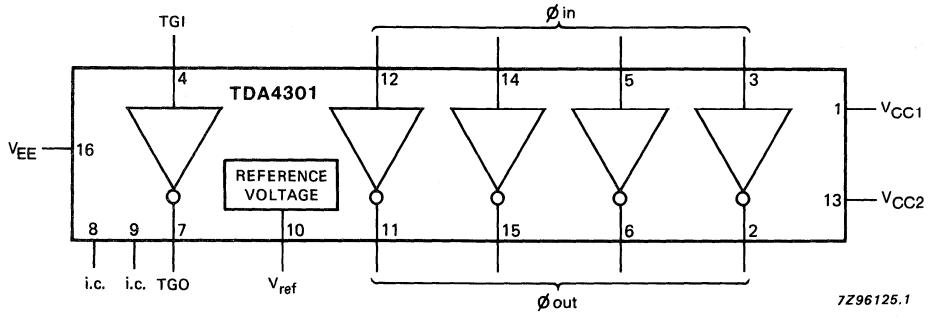


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltages					
pin 1		V_{CC1}	–	12	V
pin 13		V_{CC2}	–	12	V
DC output current	$t < 1$ s				
pins 2, 6, 11 and 13		I_O	–	250	mA
pin 7		I_{TGO}	–	10	mA
Total power dissipation		P_{tot}	–	550	mW
Operating ambient temperature range		T_{amb}	−20	+70	°C
Storage temperature range		T_{stg}	−25	+150	°C

DC CHARACTERISTICS

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	V_{CC2}	4.5	5.0	5.5	V
Supply voltage (pin 1)	V_{CC1}	11.20	11.25	11.30	V
Reference voltage (pin 10)	V_{ref}	3.60	3.75	3.90	V
Supply current (pin 13)	I_{CC2}	–	14.0	–	mA
Operating current (pin 1)	I_{CC1}	–	9.25	–	mA

DEVELOPMENT DATA

AC CHARACTERISTICS

$V_{CC1} = V_{1-16} = 11.25$ V; $V_{CC2} = V_{13-16} = 5.0$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (pins 3, 4, 5, 12 and 14)						
Input voltage range		V_ϕ	0	–	5	V
Input threshold voltage		$V_\phi TH$	0.9	1.1	1.3	V
Input current	$V_\phi = 5$ V	I_ϕ	–	10	30	μA
Outputs (pins 2, 6, 11 and 15)	$C_L = 2000$ pF					
Output voltage swing (peak-to-peak value)		$V_{\phi(p\text{-}p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	50	70	90	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	30	50	70	ns
Output (pin 7)	$C_L = 68$ pF					
Output voltage swing (peak-to-peak value)		$V_{TGO(p\text{-}p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	70	100	120	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	50	70	90	ns

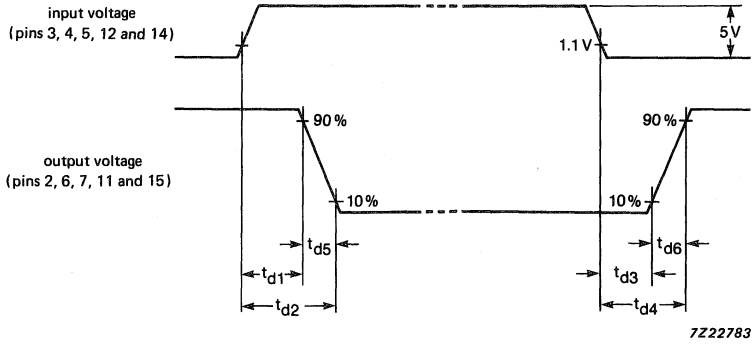


Fig.2 Timing diagram.

Load output (ϕ out) $C_L = 2000$ pF; load output (TGO) $C_L = 68$ pF. At the specified load only one switching may be done at a time.

APPLICATION INFORMATION

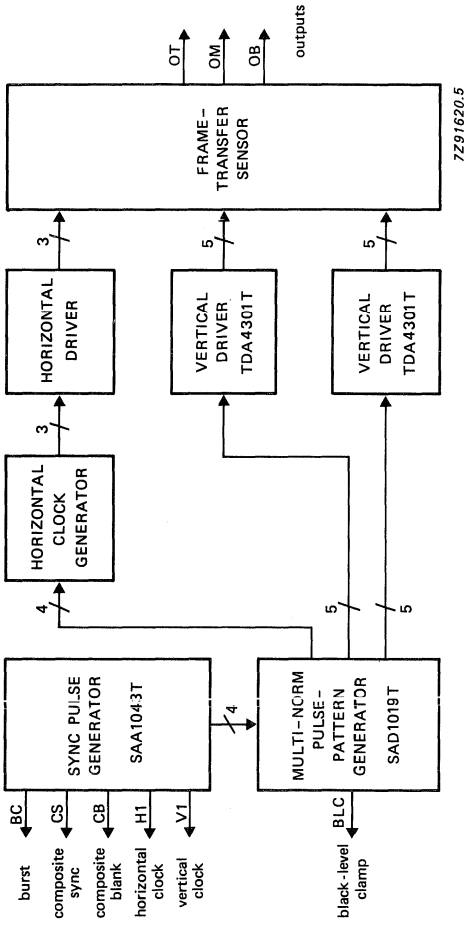


Fig.3 Control circuitry for driving the NXA1011 to NXA1041 frame-transfer sensors.

VERTICAL DRIVER

GENERAL DESCRIPTION

The TDA4301T is an integrated circuit which acts as an inverting buffer between the pulse pattern generator SAD1019 (LOCMOS technology) and the NXA1011 to NXA1041 frame transfer sensors. The circuit consists of four drivers either for all vertical transfer clocks for image part (1A to 4A), or all vertical transfer clocks for storage part (1B to 4B) electrodes, and one driver for a transfer gate (TG) electrode.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltages						
pin 11		V_{11-14}	4.5	5.0	5.5	V
pin 1		V_{1-14}	11.0	11.25	11.5	V
Supply current	V_{11-14} = 5 V	I_{11}	–	14	–	mA
Operating current	V_{1-14} = 11.25 V	I_1	–	9.25	–	mA
Storage temperature range		T_{stg}	−25	–	+150	°C
Operating ambient temperature range		T_{amb}	−20	–	+70	°C

PACKAGE OUTLINE

14-lead mini-pack; plastic (SO14; SOT108A).

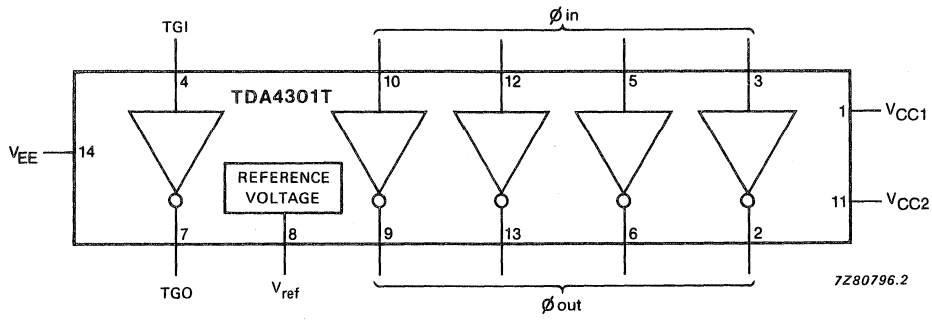


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltages					
pin 1		V_{CC1}	–	12	V
pin 11		V_{CC2}	–	12	V
DC output current	$t < 1$ s				
pins 2, 6, 9 and 13		I_O	–	250	mA
pin 7		I_{TGO}	–	10	mA
Total power dissipation		P_{tot}	–	550	mW
Operating ambient temperature range		T_{amb}	–20	+70	°C
Storage temperature range		T_{stg}	–25	+150	°C

DC CHARACTERISTICS

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 11)	V_{CC2}	4.5	5.0	5.5	V
Supply voltage (pin 1)	V_{CC1}	11.20	11.25	11.30	V
Reference voltage (pin 8)	V_{ref}	3.60	3.75	3.90	V
Supply current (pin 11)	I_{CC2}	–	14.0	–	mA
Operating current (pin 1)	I_{CC1}	–	9.25	–	mA

DEVELOPMENT DATA

AC CHARACTERISTICS

$V_{CC1} = V_{1-14} = 11.25$ V; $V_{CC2} = V_{11-14} = 5.0$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs (pins 3, 4, 5, 10 and 12)						
Input voltage range		V_ϕ	0	–	5	V
Input threshold voltage		$V_\phi TH$	0.9	1.1	1.3	V
Input current	$V_\phi = 5$ V	I_ϕ	–	10	30	μA
Outputs (pins 2, 6, 9 and 13)	$C_L = 2000$ pF					
Output voltage swing (peak-to-peak value)		$V_{\phi(p\text{-}p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	50	70	90	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	30	50	70	ns
Output (pin 7)	$C_L = 68$ pF					
Output voltage swing (peak-to-peak value)		$V_{TGO(p\text{-}p)}$	–	10	–	V
Timing	see Fig.2					
Negative slope delay		t_{d1}	–	–	100	ns
Negative slope (fall time)		t_{d5}	70	100	120	ns
Positive slope delay		t_{d3}	–	–	100	ns
Positive slope (rise time)		t_{d6}	50	70	90	ns

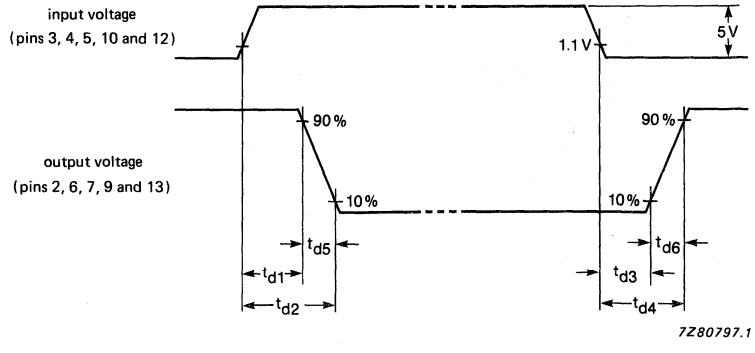


Fig.2 Timing diagram.

Load output (ϕ out) $C_L = 2000$ pF; load output (TGO) $C_L = 68$ pF. At the specified load switching only one may be done at a time.

APPLICATION INFORMATION

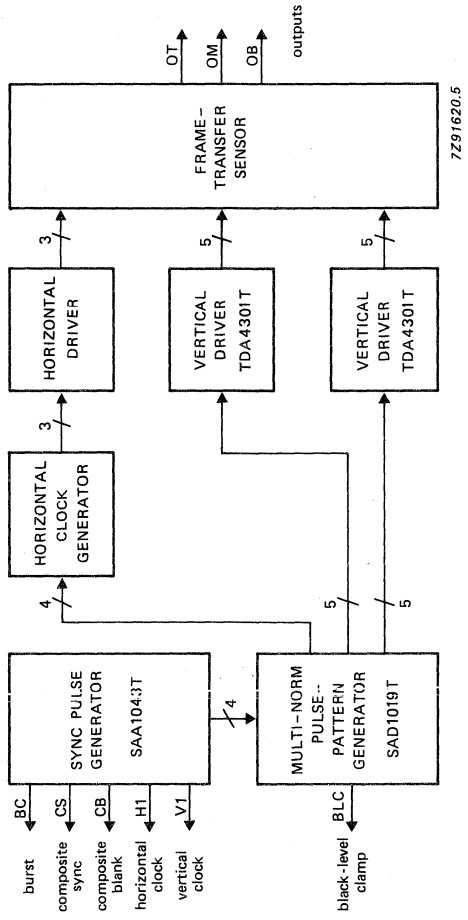


Fig.3 Control circuitry for driving the NXA1011 to NXA1041 frame-transfer sensors.

PIXEL GENERATOR

GENERAL DESCRIPTION

The TDA4302 is an integrated circuit that generates the pulses for the read-out registers of the NXA1011 to NXA1041 frame transfer sensors. The device operates in conjunction with the horizontal driver IC (TDA4305; TDA4305T).

Features

- Start.Stop RC oscillator with high accuracy over a wide temperature range
- Frequency doubler for maximum sensor drive symmetry
- Synchronous divide by 6 counter that generates the three-phase signals for the horizontal drivers
- Stop.Start oscillator controller which also selects the $\phi C'$ inputs or the divide by 6 counter outputs
- Voltage reference circuit

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 1)	$V_P = V_{1-3}$	4.5	5.0	5.5	V
Supply current (pin 1)	I_P	–	50	–	mA
Storage temperature range	T_{stg}	–25	–	+ 150	°C
Operating ambient temperature range	T_{amb}	–20	–	+ 70	°C

THIS DEVICE IS NOT RECOMMENDED FOR NEW DEVELOPMENTS

PACKAGE OUTLINES

TDA4302 : 16-lead DIL; plastic with internal heat spreader (SOT38).
TDA4302T: 16-lead mini-pack; plastic (SO16L; SOT162A).

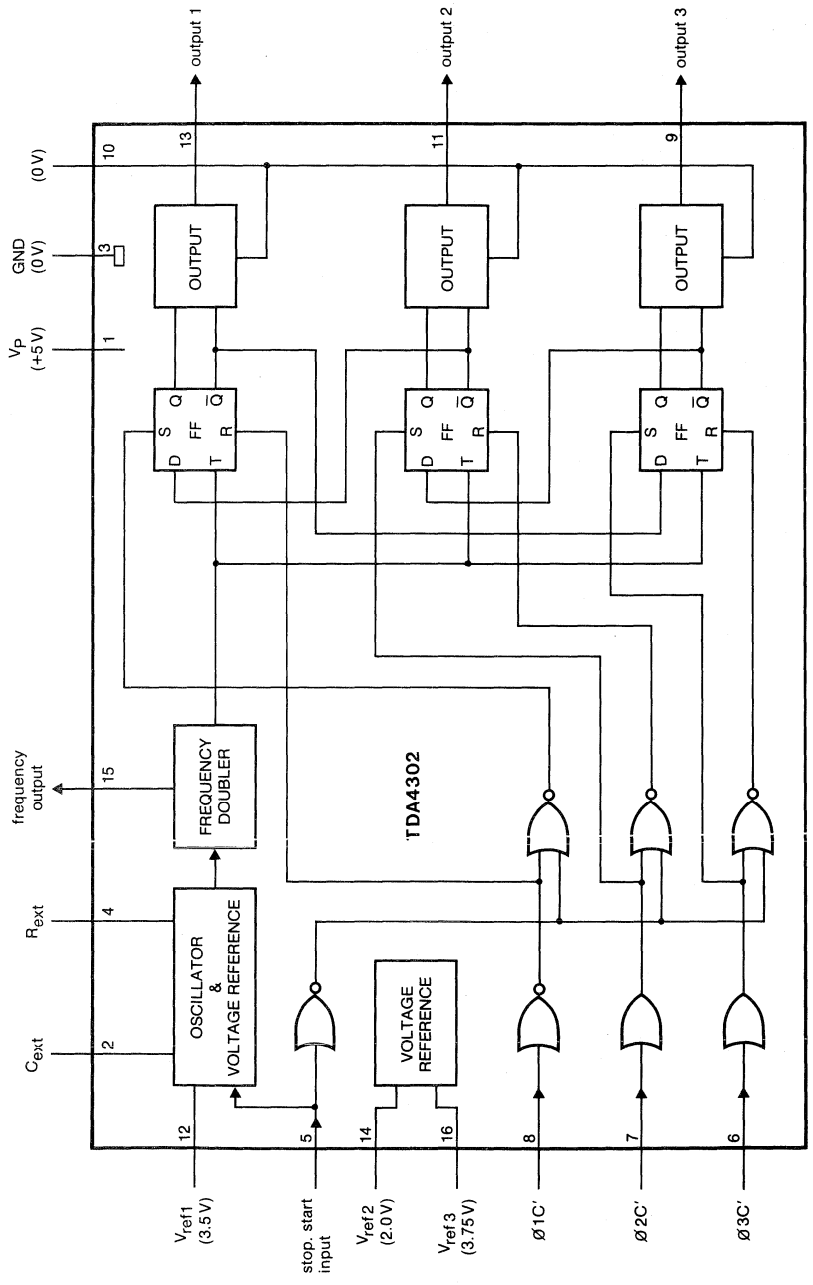


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 1)	V_P	–	12	V
Input voltage (pins 2, 4, 5, 6, 7 and 8)	V_I	–	V_P	V
Short-circuit current (DC) max. 1 s				
pin 2	I_2	–	10	mA
pin 12	I_{12}	–	100	mA
Total power dissipation				
SO package*	P_{tot}	–	340	mW
DIL package	P_{tot}	–	1000	mW
Operating ambient temperature range	T_{amb}	–20	+ 70	°C
Storage temperature range	T_{stg}	–25	+ 150	°C

* Mounted on printed-circuit board.

CHARACTERISTICS

$V_P = V_{1-3} = 5$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (pin 1)		V_P	4.5	5.0	5.5	V
Supply current (pin 1)		I_P	–	50	–	mA
Reference voltages						
3.5 V reference voltage (pin 12)	note 1	V_{ref1}	3.35	–	3.65	V
2.0 V reference voltage (pin 14)		V_{ref2}	1.9	2.0	2.1	V
3.75 V reference voltage (pin 16)		V_{ref3}	3.6	3.75	3.9	V
Source current (pins 2 and 15)		$I_{2,15}$	–	–	5	mA
Oscillator						
(C_{ext} = 100 pF; R_{ext} = 450 Ω)						
Stop.Start/HIGH: stop condition						
Stop.Start/LOW : run condition						
Output frequency (pin 15) without adjustment		f_{osc}	10.9	11.5	12.1	MHz
Frequency stability at –20 to + 60 °C			–	–	1	%
Stop.Start input (pin 5)						
Stop = 0: oscillator running	note 2					
Stop = 1: oscillator stops						
Threshold voltage		V_{5-3}	0.9	–	1.8	V
Input current	V_I – 5 V	I_5	–	–	30	μA
φC′ inputs (pins 8, 7 and 6)						
Threshold voltage		$V_{8,7,6-3}$	1.4	1.6	1.8	V
Input current	V_I = 5 V	$I_{8,7,6}$	–	–	30	μA
Outputs (pins 9, 11 and 13)						
Output voltage amplitude		$V_{9,11,13-3}$	–	1.5	–	V
Average DC output voltage		$V_{9,11,13-3}$	–	2	–	V

Notes to the characteristics

1. No DC load allowed at pin 12.
2. Extra running condition to obtain correct outputs:
   φ1C′ = HIGH (pin 8)
   φ2C′ = LOW (pin 7)
   φ3C′ = LOW (pin 6)

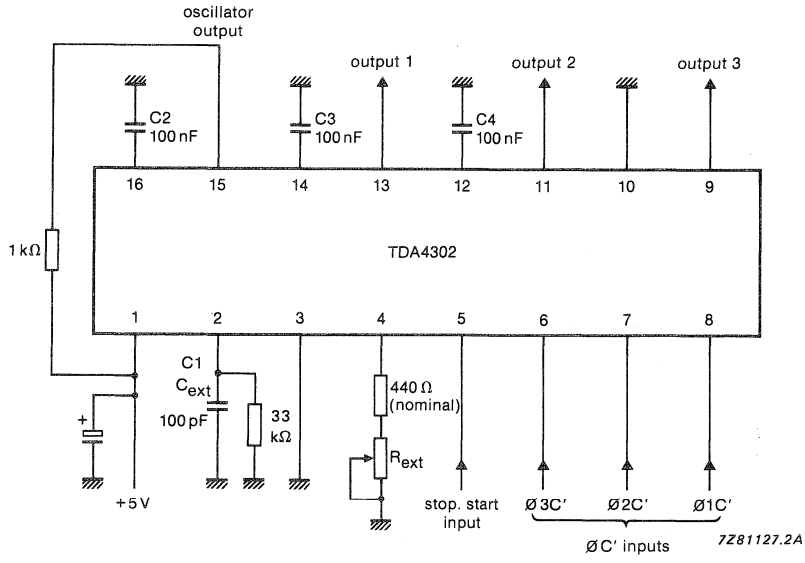


Fig.2 Application diagram.

HORIZONTAL DRIVER

GENERAL DESCRIPTION

The TDA4305 is an integrated circuit which drives the output registers of the frame transfer sensors (NXA1011to NXA1041).

Features

- Three inverting buffers
- Adjustable duty cycle control
- Voltage reference circuit

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltages					
pin 15	$V_{P1} = V_{15-6}$	4.5	5.0	5.5	V
pin 10	$V_{P2} = V_{10-6}$	11.0	11.25	11.5	V
pin 16	$V_{P3} = V_{16-6}$	11.0	11.25	11.5	V
Supply current (quiescent)					
pin 15 (outputs HIGH)	I_{P1}	–	17	–	mA
pin 15 (outputs LOW)	I_{P1}	–	8	–	mA
pin 10	I_{P2}	–	9	–	mA
pin 16	I_{P3}	–	5	–	mA
Total power dissipation	P_{tot}	–	360	–	mW
Storage temperature range	T_{stg}	–25	–	+ 150	°C
Operating ambient temperature range	T_{amb}	–20	–	+ 70	°C

THIS DEVICE IS NOT RECOMMENDED FOR NEW DEVELOPMENTS

PACKAGE OUTLINE

16-lead DIL; plastic with internal heat spreader (SOT38).

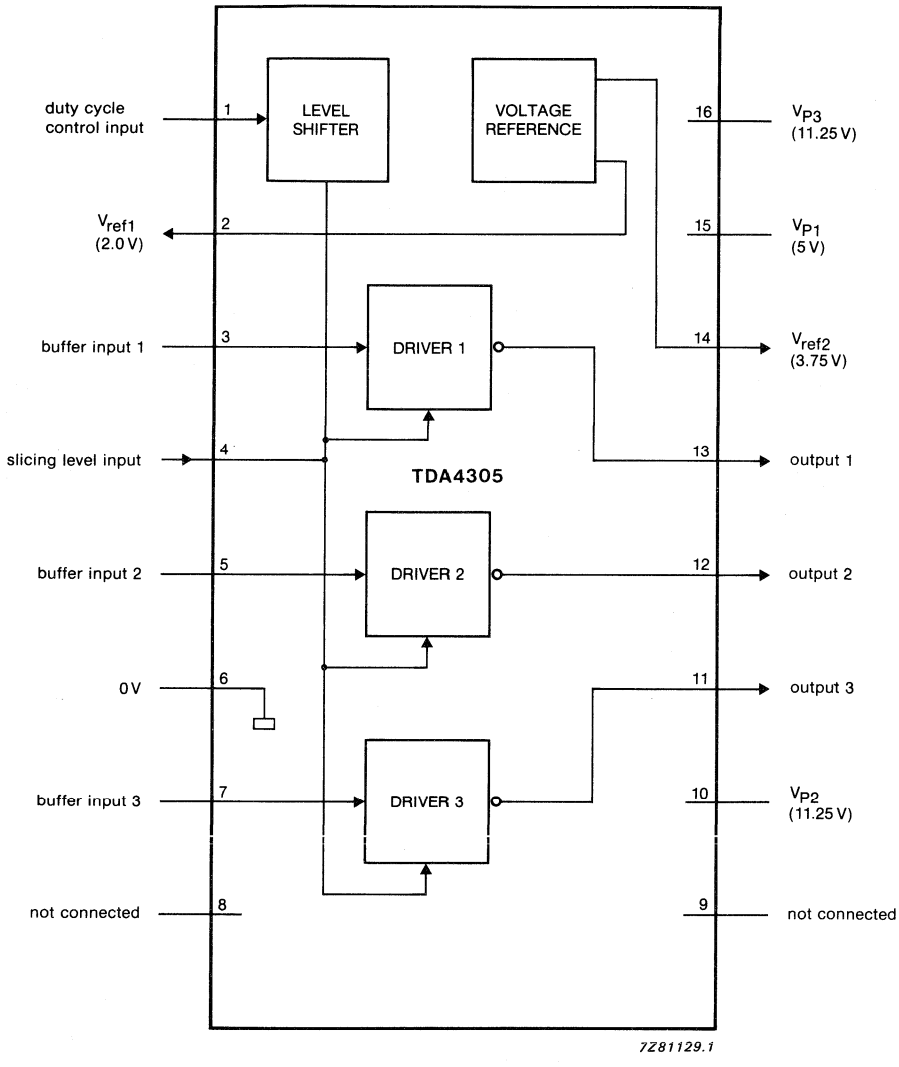


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltages				
pin 15	V_{P1}	–	12	V
pin 10	V_{P2}	–	12	V
pin 16	V_{P3}	–	12	V
Input voltage (pins 1, 3, 4, 5 and 7)	V_I	–	V_{P1}	V
Short-circuit current (pin 14)				
$t < 1$ s	I_{14}	–	1000	mA
Output current (pins 11, 12 and 13)				
$t < 1$ s	I_O	–	15	mA
Total power dissipation	P_{tot}	–	1000	mW
Operating ambient temperature range	T_{amb}	–20	+ 70	°C
Storage temperature range	T_{stg}	–25	+ 150	°C

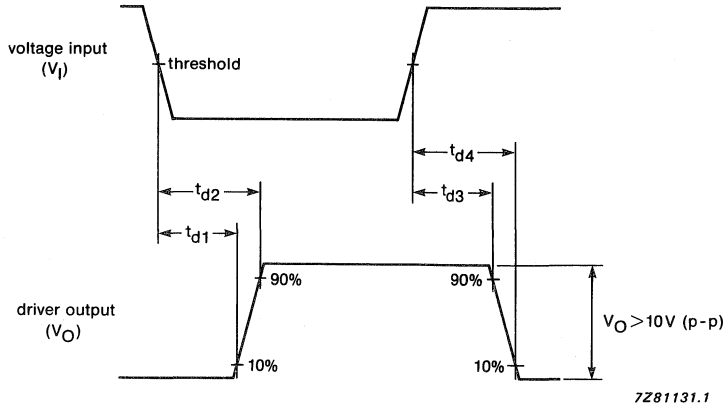
CHARACTERISTICS

$V_{P1} = V_{15-6} = 5$ V; $V_{P2} = V_{10-6} = 11.25$ V; $V_{P3} = V_{16-6} = 11.25$ V; $T_{amb} = 25\ ^{o}C$ unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
pin 15		V_{P1}	4.5	5.0	5.5	V
pin 10		V_{P2}	11.0	11.25	11.50	V
pin 16		V_{P3}	11.0	11.25	11.50	V
Supply current (quiescent)						
pin 15	outputs HIGH	I_{P1}	–	17	–	mA
pin 15	outputs LOW	I_{P1}	–	8	–	mA
pin 10		I_{P2}	–	9	–	mA
pin 16		I_{P3}	–	5	–	mA
Supply current (peak)	note 1					
pin 10	note 2	I_M	–	30	–	mA
Total power dissipation with NXA1021		P_{tot}	–	360	–	mW
Reference voltages						
2.0 V reference voltage (pin 2)		V_{ref1}	1.8	2.0	2.2	V
3.75 V reference voltage (pin 14)		V_{ref2}	3.6	3.75	3.9	V
Source current (pins 2 and 14)		$I_{2, 14}$	–	–	3	mA
Duty cycle control input (pin 1)						
Input voltage		V_{1-6}	1.75	–	2.75	V
Input current	$V_{1-6} = 2.75$ V	I_1	–	–	30	μA
Buffer inputs (pins 3, 5 and 7)						
Input current	$V_{3, 5, 7-6} = 5$ V	$I_{3, 5, 7}$	–	–	30	μA
Threshold voltage		$V_{3, 5, 7-6}$	–	2	–	V
Timing (see Fig.2)	$C_L = 68$ pF					
Rise time		t_r	20	–	40	ns
Fall time		t_f	20	–	40	ns
Delay time		t_d	–	70	100	ns
Outputs (pins 11, 12 and 13)						
Output voltage swing		$V_{11, 12, 13-6}$	–	10	–	V

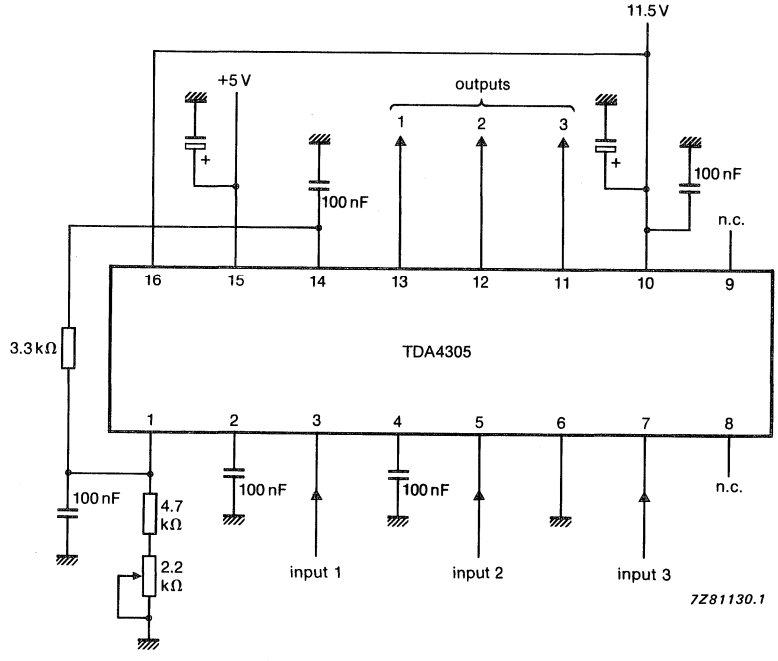
Notes to the characteristics

1. Pulses shifted 120 degrees.
2. One transition only.



Where: $t_{d1} = t_d$; $t_{d3} = t_d$; $t_{d2}-t_{d1} = t_r$; $t_{d4}-t_{d3} = t_f$.

Fig.2 Output timing.



Where: n.c. = not connected.

Fig.3 Application diagram.

HORIZONTAL DRIVER

GENERAL DESCRIPTION

The TDA4305T is an integrated circuit which drives the output registers of the frame transfer sensors (NXA1011 to NXA1041).

Features

- Three inverting buffers
- Adjustable duty cycle control
- Voltage reference circuit

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltages					
pin 13	$V_{P1} = V_{13-6}$	4.5	5.0	5.5	V
pin 8	$V_{P2} = V_{8-6}$	11.0	11.25	11.5	V
pin 14	$V_{P3} = V_{14-6}$	11.0	11.25	11.5	V
Supply current (quiescent)					
pin 13 (outputs HIGH)	I_{P1}	–	17	–	mA
pin 13 (outputs LOW)	I_{P1}	–	8	–	mA
pin 8	I_{P2}	–	9	–	mA
pin 14	I_{P3}	–	5	–	mA
Total power dissipation*	P_{tot}	–	360	–	mW
Storage temperature range	T_{stg}	–25	–	+ 150	°C
Operating ambient temperature range	T_{amb}	–20	–	+ 70	°C

* Mounted on a printed-circuit board.

THIS DEVICE IS NOT RECOMMENDED FOR NEW DEVELOPMENTS

PACKAGE OUTLINE

14-lead mini-pack; plastic (SO14; SOT108A).

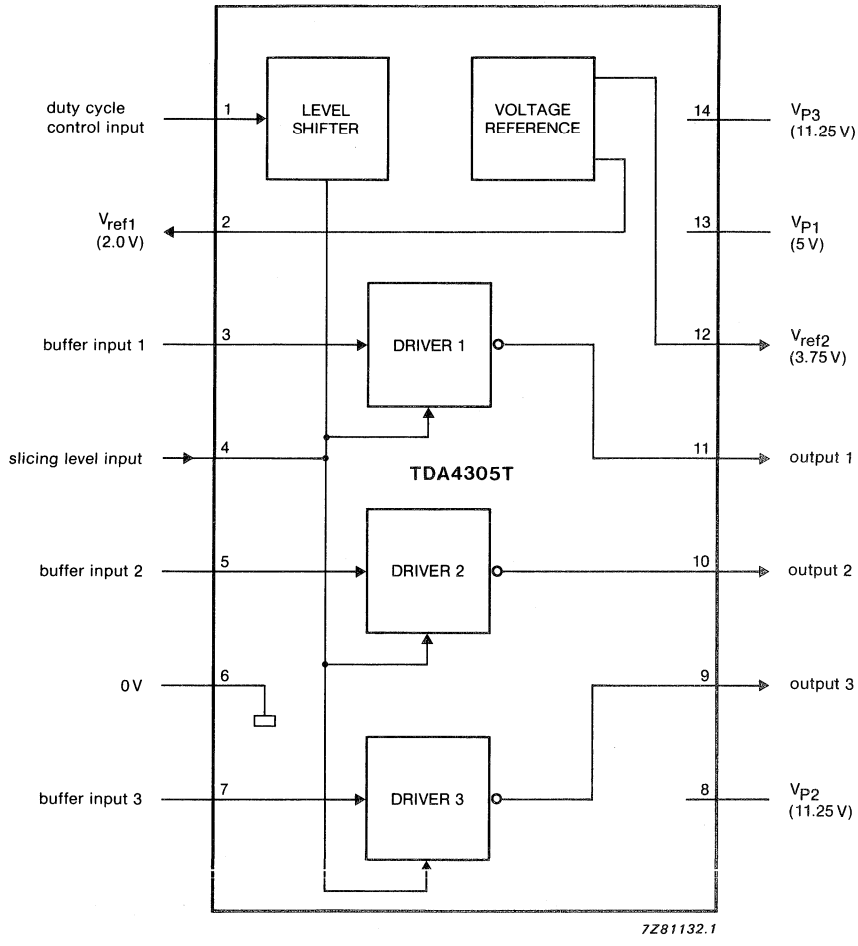


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltages				
pin 13	V_{P1}	–	12	V
pin 8	V_{P2}	–	12	V
pin 14	V_{P3}	–	12	V
Input voltage (pins 1, 3, 4, 5 and 7)	V_I	–	V_{P1}	V
Short-circuit current (pin 12)				
$t < 1$ s	I_{12}	–	100	mA
Output current (pins 9, 10 and 11)				
$t < 1$ s	I_O	–	15	mA
Total power dissipation*	P_{tot}	–	400	mW
Operating ambient temperature range	T_{amb}	–20	+ 70	°C
Storage temperature range	T_{stg}	–25	+ 150	°C

* Mounted on a printed-circuit board.

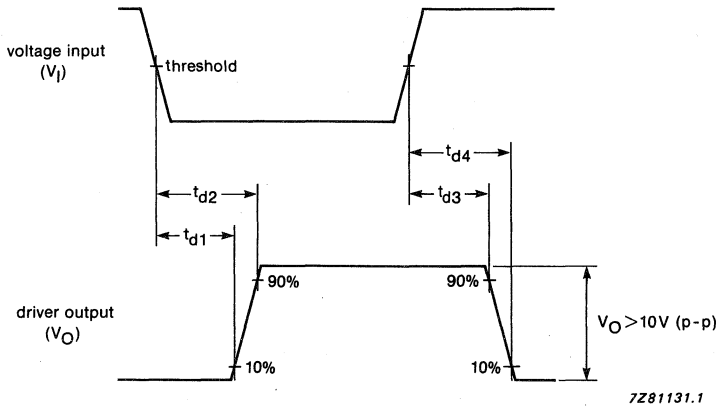
CHARACTERISTICS

$V_{P1} = V_{13-6} = 5$ V; $V_{P2} = V_{8-6} = 11.25$ V; $V_{P3} = V_{14-6} = 11.25$ V; $T_{amb} = 25$ °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage						
pin 13		V_{P1}	4.5	5.0	5.5	V
pin 8		V_{P2}	11.0	11.25	11.50	V
pin 14		V_{P3}	11.0	11.25	11.50	V
Supply current (quiescent)						
pin 13	outputs HIGH	I_{P1}	–	17	–	mA
pin 13	outputs LOW	I_{P1}	–	8	–	mA
pin 8		I_{P2}	–	9	–	mA
pin 14		I_{P3}	–	5	–	mA
Supply current (peak)	note 1					
pin 10	note 2	I_M	–	30	–	mA
Total power dissipation with NXA1021		P_{tot}	–	360	–	mW
Reference voltages						
2.0 V reference voltage (pin 2)		V_{ref1}	1.8	2.0	2.2	V
3.75 V reference voltage (pin 12)		V_{ref2}	3.6	3.75	3.9	V
Source current (pins 2 and 12)		$I_{2,12}$	–	–	3	mA
Duty cycle control input (pin 1)						
Input voltage		V_{1-6}	1.75	–	2.75	V
Input current	$V_{1-6} = 2.75$ V	I_1	–	–	30	μA
Buffer inputs (pins 3, 5 and 7)						
Input current	$V_{3,5,7-6} = 5$ V	$I_{3,5,7}$	–	–	30	μA
Threshold voltage		$V_{3,5,7-6}$	–	2	–	V
Timing (see Fig.2)	$C_L = 68$ pF					
Rise time		t_r	20	–	40	ns
Fall time		t_f	20	–	40	ns
Delay time		t_d	–	70	100	ns
Outputs (pins 9, 10 and 11)						
Output voltage swing		$V_{9,10,11-6}$	–	10	–	V

Notes to the characteristics

1. Pulses shifted 120 degrees.
2. One transition only.



Where: $t_{d1} = t_d$; $t_{d3} = t_d$; $t_{d2}-t_{d1} = t_r$; $t_{d4}-t_{d3} = t_f$.

Fig.2 Output timing.

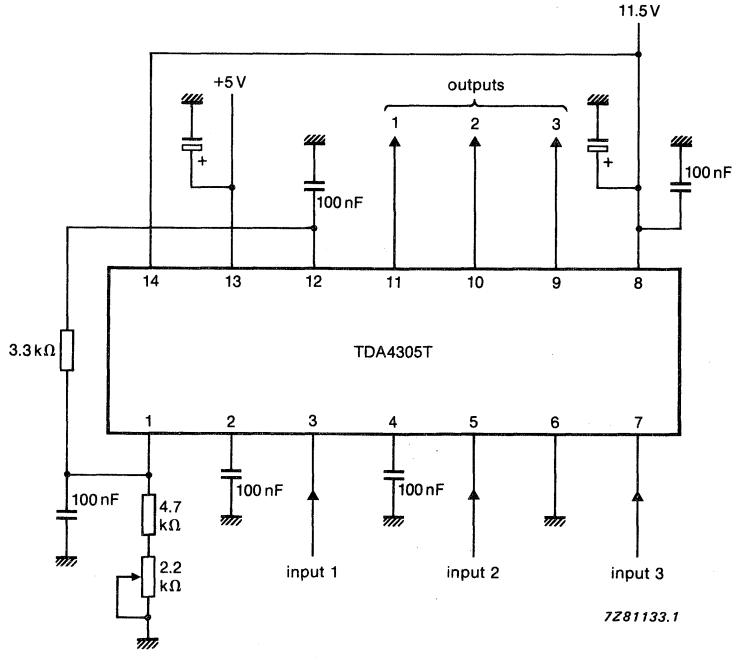


Fig.3 Application diagram.

Video Processing ICs

PAL – NTSC ENCODER

GENERAL DESCRIPTION

The TDA2501 encodes two colour-difference signals R-Y and B-Y onto one subcarrier. Quadrature modulation allows the coding to be in accordance with either the PAL or NTSC system.

Features

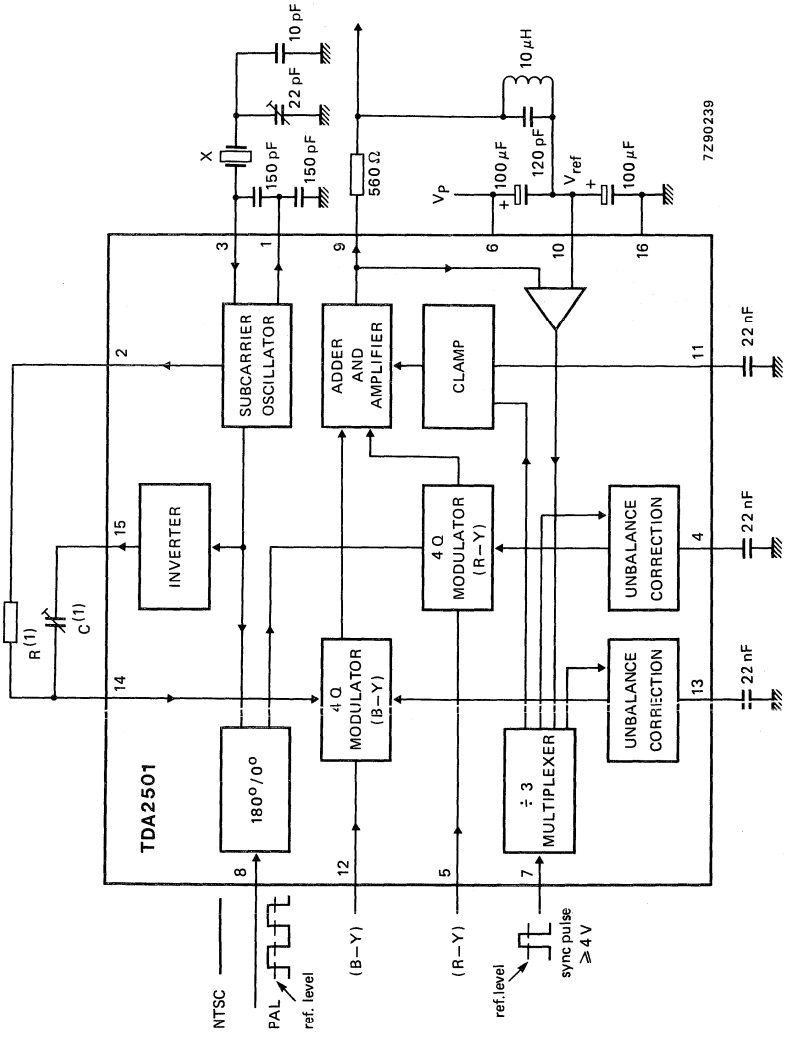
- Generates two sinusoidal subcarriers with a relative phase of 90° (also accepts external subcarriers)
- Modulates the two subcarriers with the colour difference signals
- Inverts the output from one modulator on command of an external signal (as in case of PAL)
- Sums the output from the modulators to obtain a quadrature modulated output signal
- Clamps the output DC level to a reference voltage
- Divides the frequency of horizontal sync pulses by three so that the output level can be clamped and the balance of the two modulators sequentially controlled during the line-blanking minus burst-key period

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage range (pin 6)	V_P	5.5	6.8	10	V
Supply current range (pin 6)	I_P	28	40	64	mA
Chrominance output voltage (pin 9) (peak-to-peak value)	$V_{9(p\text{-}p)}$	–	–	1.4	V
Operating ambient temperature range	T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

TDA2501 : 16-lead DIL; plastic (with internal heat spreader) (SOT38).
TDA2501T: 16-lead mini-pack; plastic (SO16L; SOT162A).



(1) R = 0.885 (2 π fC); for PAL f = 4.433 619 MHz, R = 963 Ω and C = 33 pF.

Fig.1 Block diagram; also test and application diagram.

DESCRIPTION

The colour difference signals B-Y and R-Y with a maximum amplitude of 1.4 volt are to be applied at pin 12 and pin 5. DC-coupling of the input signals is allowed if their DC levels are within specified limits from the DC level at pin 10 (V_{ref}). The following table shows these limits as a function of supply voltage. The table also shows the limits of the reference voltage range as a function of the supply voltage.

supply voltage V_{6-16} (V)	input DC (R-Y) (B-Y) min. (V)*	V_{5-16} V_{12-16} (V) max. (V)**	reference voltage ▲ V_{10-16} (V)		
			min	typ.	max.
5.5	2.4	3.3	2.3	3.0	3.5
6.0	$> V_{ref} - 1.4$ V	3.8	2.4	3.3	3.9
7.0	$> V_{ref} - 1.4$ V	4.8	2.6	4.0	4.7
8.0	$> V_{ref} - 1.4$ V	5.8	2.8	4.8	5.5
9.0	$> V_{ref} - 1.4$ V	6.8	3.0	5.5	6.3
10.0	$> V_{ref} - 1.4$ V	7.8	3.2	6.3	7.1

* Minimum 2.4 V.
** At $V_S - 2.2$ V.
▲ Minimum values at $0.2\ V_S + 1.2$ V.
Typical values without pull-up or pull-down resistor.
Maximum values at $0.8\ V_S - 0.9$ V.

The inputs (B-Y) and (R-Y) should be zero, independent of their (limited) DC-levels, during the line-blanking minus burst-key period (LB – BK). Clamping the output and correcting the out-of-balance of the modulators, is achieved by applying a HIGH level to pin 7 within the (LB–BK) period (e.g. line sync pulse).

Modulation at output:
V_8 = LOW; output = sc x (B-Y) + sc' x (R-Y)
V_8 = HIGH; output = sc x (B-Y) – sc' x (R-Y)
in which sc' = subcarrier
sc = 90° phase-shifted subcarrier to sc' (sc lags).

The bandpass filter at the output suppresses the DC components of the (R-Y) + (B-Y) signal. Luminance (Y) is not processed by this circuit.

Internal subcarrier

The internal subcarrier oscillator is crystal controlled. The oscillator generates a sinewave with low harmonic distortion and an amplitude of about 500 mV peak-to-peak. The amplitude can be changed if necessary with a current input at pin 1. The adjustment range is 0 to 800 mV, with a corresponding current range of +250 to –150 μA.

Phase shift

To obtain a 90° phase-shifted carrier, two low impedance subcarrier outputs are provided, pins 2 and 15, the last being the inverse of the first. Between pins 2 and 15 an external RC combination must be used to obtain the desired 90° shift. The capacitor value must be limited to 33 pF to minimize subcarrier distortion.

The resistor required between pins 2 and 14 is $0.885\ (2\ \pi\ fC)$.

External subcarrier

The (B-Y) and (R-Y) signals can also be multiplied with an external subcarrier. In this event the external subcarrier is connected to pin 1. For maximum input impedance at pin 1 $V_3 = V_{16}$ ($Z_{mi} > 1400\ \Omega$). The same RC network generates the 90° phase-shifted subcarrier. For the use of an externally generated subcarrier, applied at pin 14, the DC level must be the same as that of an RC-network generated one.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 6 to pin 16)	V_P	–	13.2	V
Total power dissipation	P_{tot}	see Fig.2		W
Operating ambient temperature range	T_{amb}	−25	+70	°C
Storage temperature range	T_{stg}	−65	+150	°C

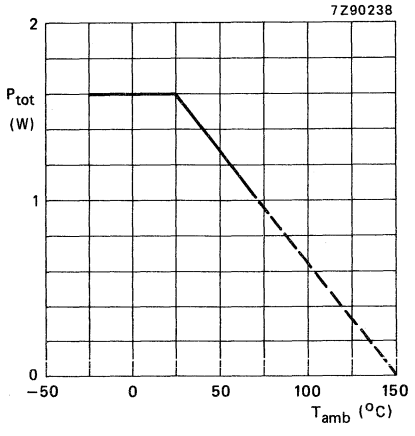


Fig.2 Power derating curve.

CHARACTERISTICS

$V_P = V_{6-10} = -V_{16-10} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Single supply voltage	V_{6-16}	5.5	6.8	10	V
Dual supply voltage					
positive (pin 6)	V_{6-10}	2.0	3.0	5.0	V
negative (pin 16)	$-V_{16-10}$	2.3	3.0	5.0	V
Supply current (pin 10)	I_{10}	−1	0	3.5	mA
positive (pin 6)	I_6	28	40	64	mA
negative (pin 16)	$-I_{16}$	28	40	64	mA
Limitation DC level					
oscillator feedback	V_1	−30	0	+30	mV
Nominal amplitude input signal (peak-to-peak value)					
pin 5	$V_{5(p-p)}$	–	1	1.4	V
pin 12	$V_{12(p-p)}$	–	1	1.4	V
Input voltages (R-Y) and (B-Y) zero DC level					
pin 5	V_5	2.4	3.3	3.9	V
pin 12	V_{12}	2.4	3.3	3.9	V
Required level of sync input					
HIGH	V_7	4	–	V_P	V
LOW	V_7	–	–	V_{10}	V
Required level of PAL pulse (H/2)					
HIGH	V_8	$V_{10}+0.8$	–	V_P	V
LOW	V_8	$-V_P$	–	0	V
Sync input current					
$V_7 = V_P + 1$ V	I_7	–	4	15	μA
PAL input current (H/2)					
$V_8 = V_{10} + 0.8$ V	I_8	–	1.5	5	μA
Chrominance output voltage swing (R-Y) = (B-Y) = 1.4 V; subcarrier pulse = 0.5 V (peak-to-peak value)	$V_{9(p-p)}$	–	–	1.4	V
Amplitude of suppressed subcarrier	V_9	0	7	16	mV
Input currents					
$V_4 = V_{10}$	I_4	0	1.5	5	μA
$V_{11} = V_{10}$	I_{11}	0	1.5	5	μA
$V_{13} = V_{10}$	I_{13}	0	1.5	5	μA
$V_5 = V_{10}$	I_5	0	9	30	μA
$V_{12} = V_{10}$	I_{12}	0	9	30	μA
$V_{14} = V_{16} + 2.3$ V	I_{14}	–	6	–	μA
Input impedance					
(R-Y)	Z_5	–	160	–	kΩ
(B-Y)	Z_{12}	–	160	–	kΩ

SECAM ENCODER

GENERAL DESCRIPTION

The TDA2506 converts colour-difference signals (D'_R and D'_B) into sequential, frequency modulated signals according to the SECAM system. The signals (D'_R) and (D'_B) are the colour difference signals before low-frequency pre-emphasis; D'_R = -1,9 (R-Y) and D'_B = +1,5(B-Y). The circuit is intended for use in video cameras, games, recorders and players, PAL-SECAM transcoding circuits and SECAM test signal generators.

Synchronizing pulses required for operation of the TDA2506 may be obtained from a universal sync generator SAA1043 or other pulse generator. All pulses are to be active HIGH and are as follows:

Horizontal sync pulses to pin 11
Half-rate horizontal sync (H/2) pulses to pin 9
Vertical sync pulses to pin 12
Chrominance blanking pulses to pin 13 (may include colour-killer pulses)

Frequency modulation is performed in conjunction with modulator-controller TDA2507.

Features

- Chrominance processor
- Vertical identification signal generator
- Timing pulse output to TDA2507
- Sample and hold circuit for control signal from TDA2507
- No adjustments of external components required (except high-frequency pre-emphasis (bell filter) stage)

QUICK REFERENCE DATA

Supply voltage	V_{4-2}	typ.	5 V
Supply current	I_4	typ.	45 mA
Reference voltage	V_{7-2}, V_{22-24}	typ.	3,5 V
Operating ambient temperature range	T_{amb}		−25 to +70 °C
Storage temperature range	T_{stg}		−65 to +150 °C

PACKAGE OUTLINES

24-lead DIL; plastic (with internal heat spreader) (SOT-101B).

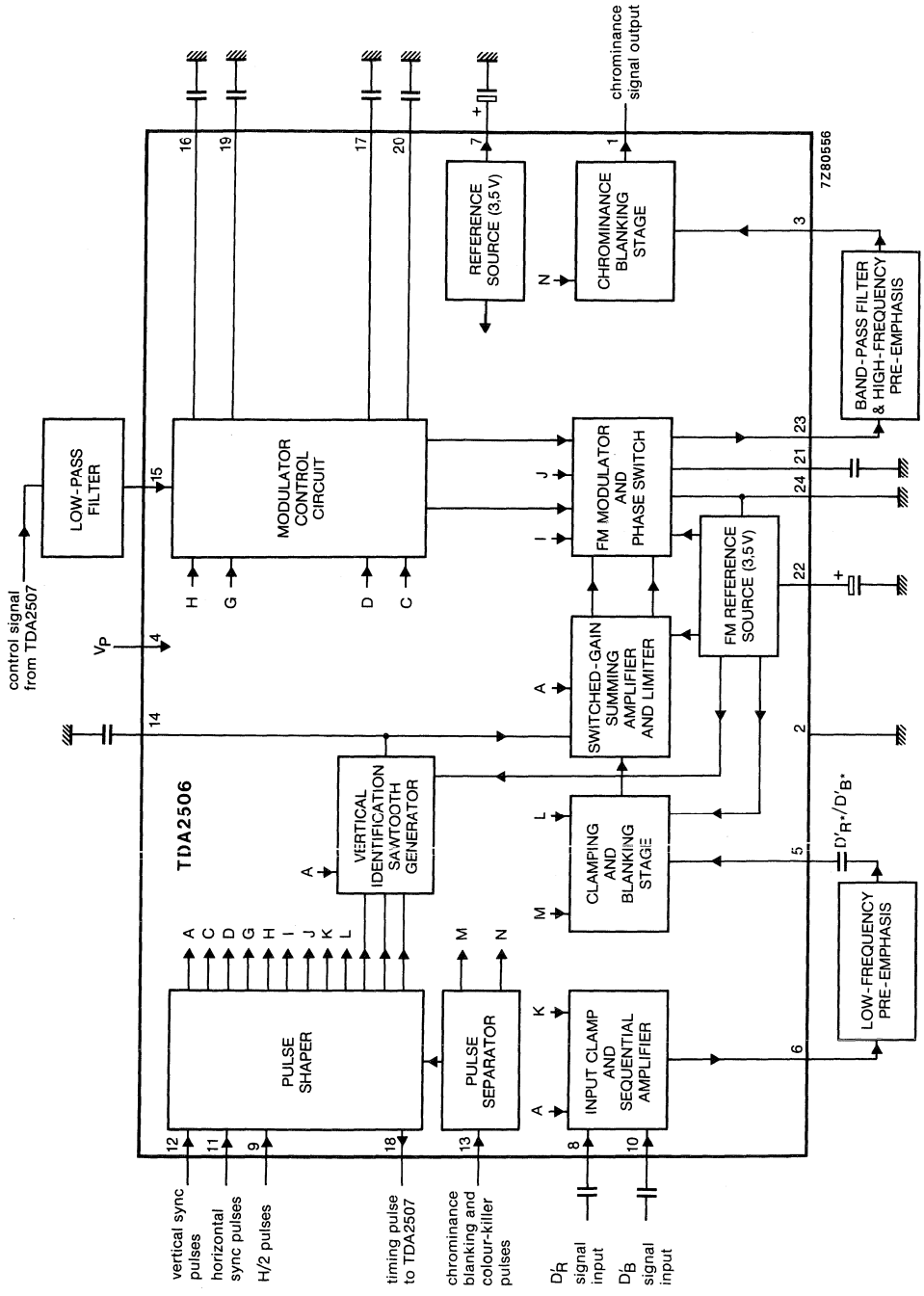


Fig. 1 Block diagram.

Pin functions

1. Chrominance signal output.
2. Ground.
3. Input to chrominance blanking stage from high-frequency pre-emphasis and band-pass filter.
4. Positive supply voltage.
5. Input to clamping and blanking stage from low-frequency pre-emphasis filter.
6. Output from sequential amplifier to low-frequency pre-emphasis filter.
7. Reference voltage output.
8. D'_R signal input.
9. H/2 pulse input (required only if specific phase sequencing is desired).
10. D'_B signal input.
11. Horizontal sync pulse input.
12. Vertical sync pulse input.
13. Chrominance blanking and colour-killer pulse input.
14. Capacitor for vertical identification sawtooth.
15. Control signal input from TDA2507 via low-pass filter.
16. 4 406,250 kHz frequency adjustment.
17. (R-Y) control.
18. Timing pulse output to TDA2507.
19. 4 250,000 kHz frequency adjustment.
20. (B-Y) control.
21. FM modulator tuning capacitor (fixed).
22. FM reference voltage output.
23. FM modulator output to high frequency pre-emphasis and band-pass filter.
24. Ground connection for FM modulator.

FUNCTIONAL DESCRIPTION

Input clamp and sequential amplifier

This circuit clamps the zero levels of the D'_R and D'_B input signals (pins 8 and 10) to the reference voltage from pin 7. The input signals are switched into the amplifier sequentially by an internally delayed H/2 waveform. The amplifier output at pin 6 is D'_R when the delayed H/2 waveform is HIGH and D'_B when it is LOW. The stage gain is 1,5.

Clamping and blanking stage

After external low-frequency pre-emphasis, the sequential $D'_R{}^*$ and $D'_B{}^*$ signals are returned to the IC at pin 5. The signal amplitude at pin 5 is typically 0,5 V (peak-to-peak value) for 75% colour bar (EBU). Black levels are clamped to the FM reference voltage (pin 22). Blanking takes place during the chrominance blanking pulse and, if required, during the video blanking and/or colour killing pulses.

FUNCTIONAL DESCRIPTION (continued)

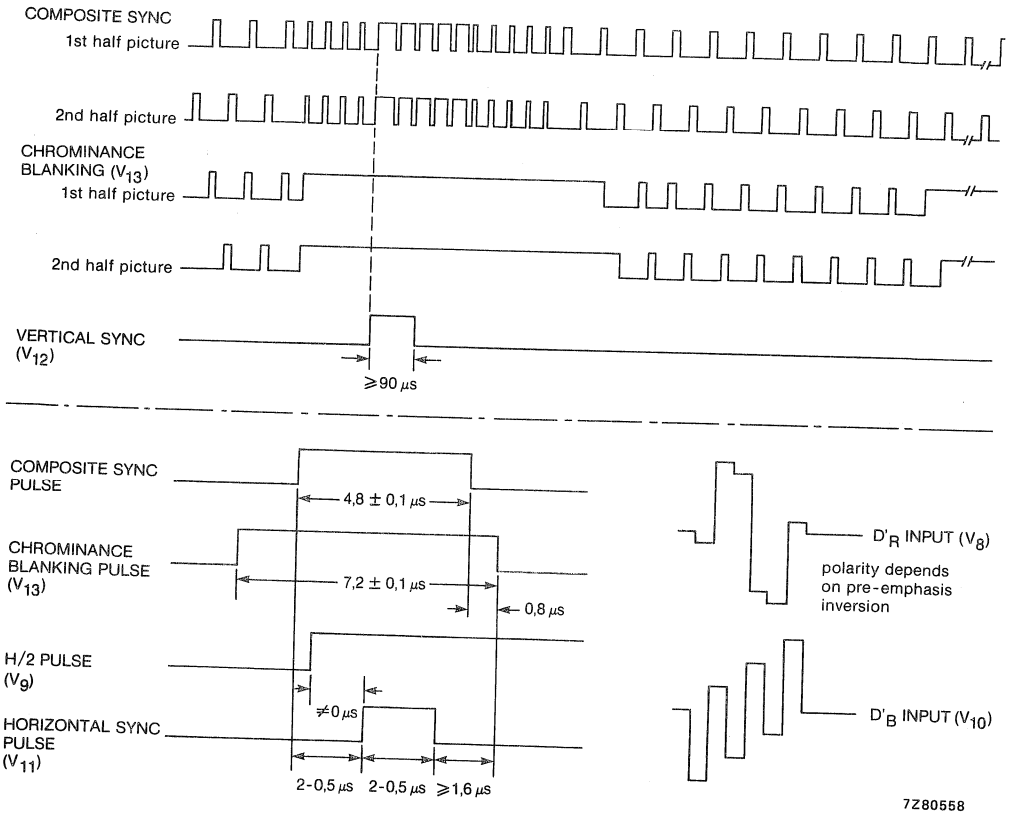


Fig. 2 Survey of input signals in relation to composite sync.

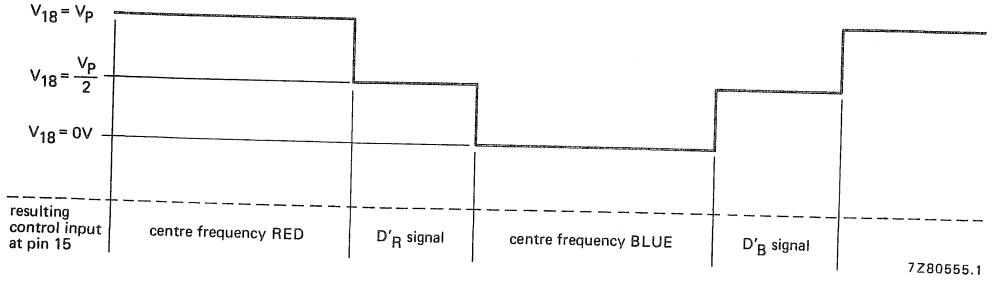


Fig. 3 Timing pulse output (pin 18) and resulting control input (pin 15).

Switched-gain summing amplifier and limiter

Inputs into the summing amplifier are the sequential D'_R* and D'_B* signals, the vertical identification sawtooth waveform and reference d.c. levels. The gain of the amplifier is switched by the internally delayed H/2 waveform to give the correct input amplitudes for the FM modulator (D'_R* gain = 280/230 x D'_B* gain). An offset is also introduced between the black levels of the D'_R* and D'_B* signals which corresponds to the upper and lower thresholds of the limiter.

FM modulator and phase switch

The FM modulator provides accurate FM modulation which follows the amplitude envelopes of the sequential D'_R* and D'_B* waveforms. The centre frequencies of 4 406,250 kHz for the D'_R* signal and 4 250,000 kHz for the D'_B* signal are controlled by d.c. levels from the sample and hold circuit (which in turn are controlled by the TDA2507). The upper and lower frequency limits are 4 756,000 ± 35 kHz and 3 900,000 ± 35 kHz.

Reference d.c. levels are switched within the FM modulator to define the starting phase of the modulator output (pin 23) at the initiation of each horizontal and vertical scan. The starting phase sequence is as follows:

vertical scan (frame to frame) 0^o, 180^o, 0^o, 180^o, repeating;

horizontal scan (line to line) 0^o, 0^o, 180^o, 0^o, 0^o, 180^o, repeating.

Chrominance blanking stage

The frequency modulated colour difference signals are passed via high-frequency pre-emphasis and band-pass filters to the chrominance blanking input at pin 3. The d.c. level of this input should be equal to the reference voltage at pin 7. Blanking occurs during the chrominance blanking pulse. The stage gain is 1,75.

Vertical identification sawtooth generator

Vertical sync, horizontal sync and chrominance blanking pulses are used to determine vertical identification (see Fig. 4). The vertical identification sawtooth generator is driven in opposite directions for identification signals IdR and IdB; the capacitor for the generator is connected at pin 14. If no vertical identification is required, pin 14 should be connected to the FM reference voltage at pin 22.

Pulse shaper

This stage developes all pulses that are required within the TDA2506 and also the timing pulses required for the modulator controller TDA2507 (see Fig. 3). Internal H/2 pulses are generated by a flip-flop working from the horizontal sync input (pin 11), this makes the H/2 input at pin 9 necessary only if it is required to lock the modulator into a specific phase sequence. If the H/2 input is not required, pin 9 should be connected to ground. A pulse separator at the chrominance blanking/colour-killer input (pin 13) allows this input to be used for blanking the sequential D'_R*/D'_B* signal.

Sample and hold circuit

This circuit provides reference voltages to the FM modulator which set the centre modulation frequencies for the sequential D'_R* and D'_B* signals. The reference voltage levels are supplied to pin 15 from the TDA2507 in a sequence that is time-related to D'_R*/D'_B* switching. The levels are sampled and then held for D'_R* using capacitors at pins 16 and 17, and for D'_B* using capacitors at pins 19 and 20.

FUNCTIONAL DESCRIPTION (continued)

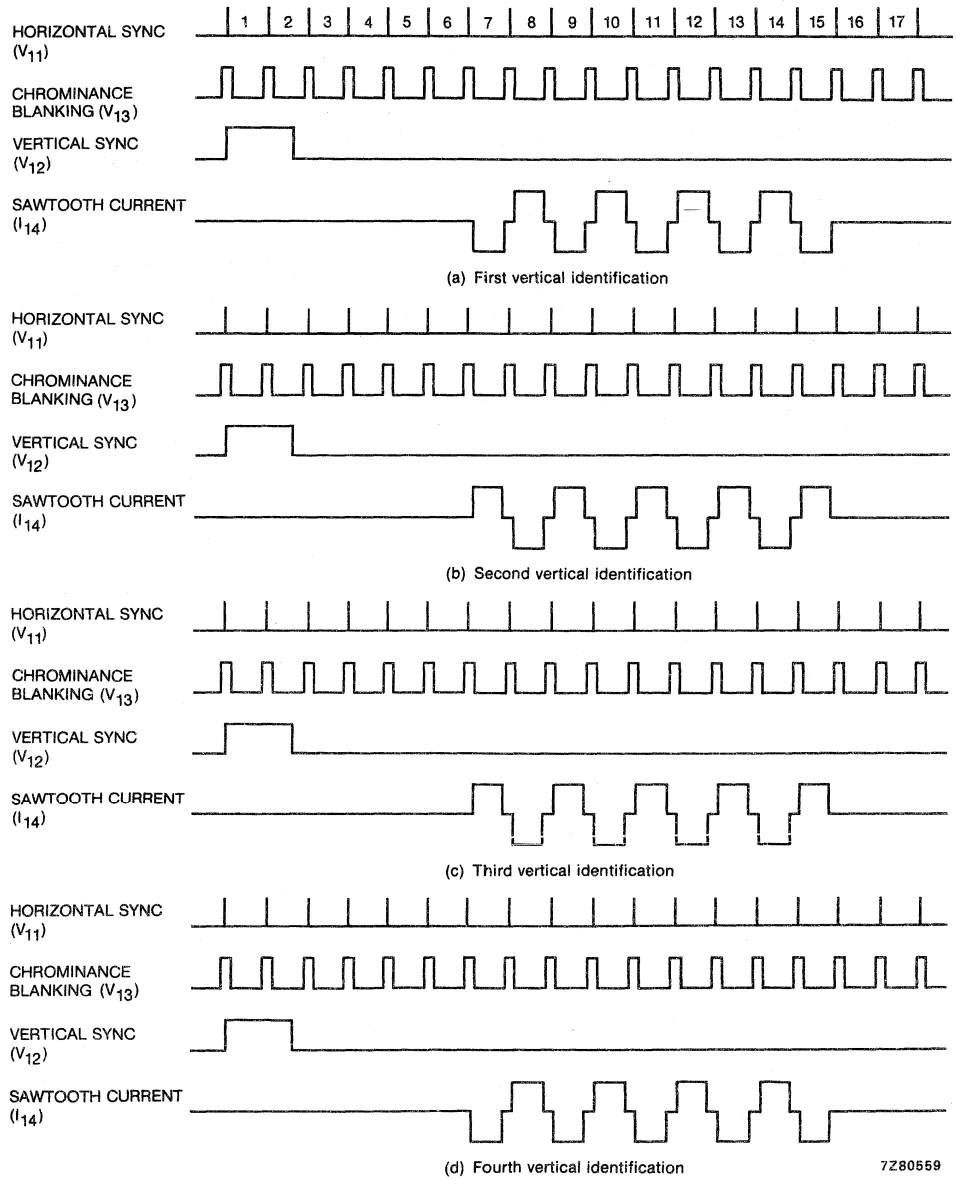


Fig. 4 Vertical identification generation.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating system IEC 134

Supply voltage	V_{4-1}	max. 13,2 V
Total power dissipation	P_{tot}	see Figs 5 and 6
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−65 to +150 °C

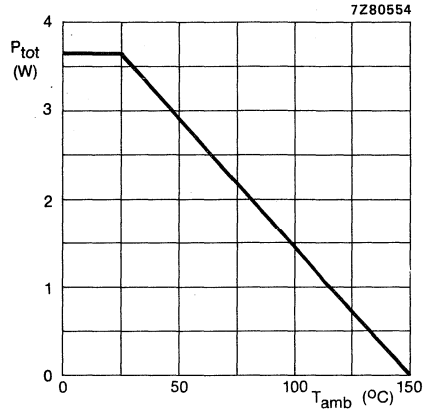


Fig. 5 Power derating curve for DIL package (SOT-101B).

CHARACTERISTICS

$V_p = V_{4-2} = 5$ V; $T_{amb} = 25$ °C; all voltages are with reference to ground (pins 2 and 24); all currents stated are positive into the IC; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 4)	$V_p = V_{4-2}$	4,75	5	7	V
Supply current	$I_p = I_4$	30	45	60	mA
Reference voltage (pin 7)	V_{7-2}	3,35	3,5	3,65	V
Reference voltage (pin 22)	V_{22-24}	3,35	3,5	3,65	V
Pulse shaper (pins 9,11 and 12, emitter follower inputs; pin 18, collector output)					
Bias current (pin 9,11,12)	I_9, I_{11}, I_{12}	–	–	10	μA
Input resistance (pin 9,11,12)	R_9, R_{11}, R_{12}	200	–	–	kΩ
Input pulse amplitude (pin 9,11,12)	V_9, V_{11}, V_{12}	2	–	–	V
Timing pulse output (pin 18) high level	V_{18}	4,7	–	–	V
intermediate ($V_p/2$) level	V_{18}	2,3	–	2,7	V
low level	V_{18}	–	–	0,3	V
Pulse separator (pin 13, emitter follower)					
Input resistance	R_{13}	100	–	–	kΩ
Chrominance blanking pulse amplitude	V_{13}	3,6	–	–	V
D'_R*/D'_B* blanking pulse amplitude (colour killing)	V_{13}	1,7	1,8	1,9	V
Vertical identification sawtooth generator (pin 14)					
Voltage clamping level	V_{14}	V_{22}–7 mV	V_{22}	V_{22}+7 mV	V
Ramp current (occurs in lines 7 to 15 after vertical sync)	$\pm I_{14}$	50	70	85	μA
Maximum voltage level	V_{14}	V_{22}+0,6	V_{22}+0,7	V_{22}+0,8	V
Minimum voltage level	V_{14}	V_{22}–0,8	V_{22}–0,7	V_{22}–0,6	V
Voltage level during line blanking	V_{14}	V_{22}–7 mV	V_{22}	V_{22}+7 mV	V
Inputs D'_R*, D'_B* (pins 8 and 10)					
Signal level during clamping ($I_8, I_{10} = \pm 50$ μA)	V_8, V_{10}	V_7–20 mV	V7	V_7+20 mV	V
Input bias current	I_8, I_{10}	–	–	1,5	μA

parameter	symbol	min.	typ.	max.	unit
Sequential amplifier output (pin 6)					
(Pins 8 and 10 a.c. coupled to fixed d.c. voltage)					
D.C. output	V_6	1,6	$\frac{V_7}{2}$ – 10 mV	1,85	V
Output resistance	R_6	–	12	16	Ω
Amplifier voltage gain (pin 8 or 10 to pin 6)	$G_{8,10\text{-}6}$	1,46	1,5	1,54	
Clamping and blanking stage (pin 5)					
Input voltage (clamped; $I_5 = \pm 50\ \mu A$)	V_5	V_{22} – 10 mV	V_{22}	V_{22} + 10 mV	V
Input bias current	I_5	–	–	1,0	μA
Modulator control circuit (pin 15, buffer amplifier non-inverting input)					
Bias current	I_{15}	–	–	1,25	μA
Permitted input signal d.c. levels	V_{15}	2	–	4,3	V
FM modulator output (pin 23, emitter follower)					
Output resistance	R_{23}	–	50	70	Ω
High d.c. output level at $V_{21} = 4$ V	V_{23}	V_{22} – 0,85	–	V_{22} – 0,7	V
Output signal amplitude	V_{23}	0,9	1,0	1,1	V

CHARACTERISTICS (Continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance blanking stage (pin 3, emitter follower input; pin 1, amplifier output)					
Input current	I_3	–	–	15	μA
Input resistance	R_3	300	–	–	kΩ
Required d.c. level of input signal	V_3	–	V_7	–	V
Output resistance	R_1	–	–	5	Ω
Temperature coefficient of output d.c. level	TC	–	1,8	—	mV/K
Amplifier gain	G_{3-1}	1,70	1,75	1,80	
Output d.c. level during blanking(V_{13} = HIGH)	V_1	V_7–0,76	V_7–0,70	V_7–0,60	V
Output d.c. level unblanked ($V_3 = V_7$; V_{13} = LOW)	V_1	V_7–0,76	V_7–0,70	V_7–0,60	V

A.C. CHARACTERISTICS

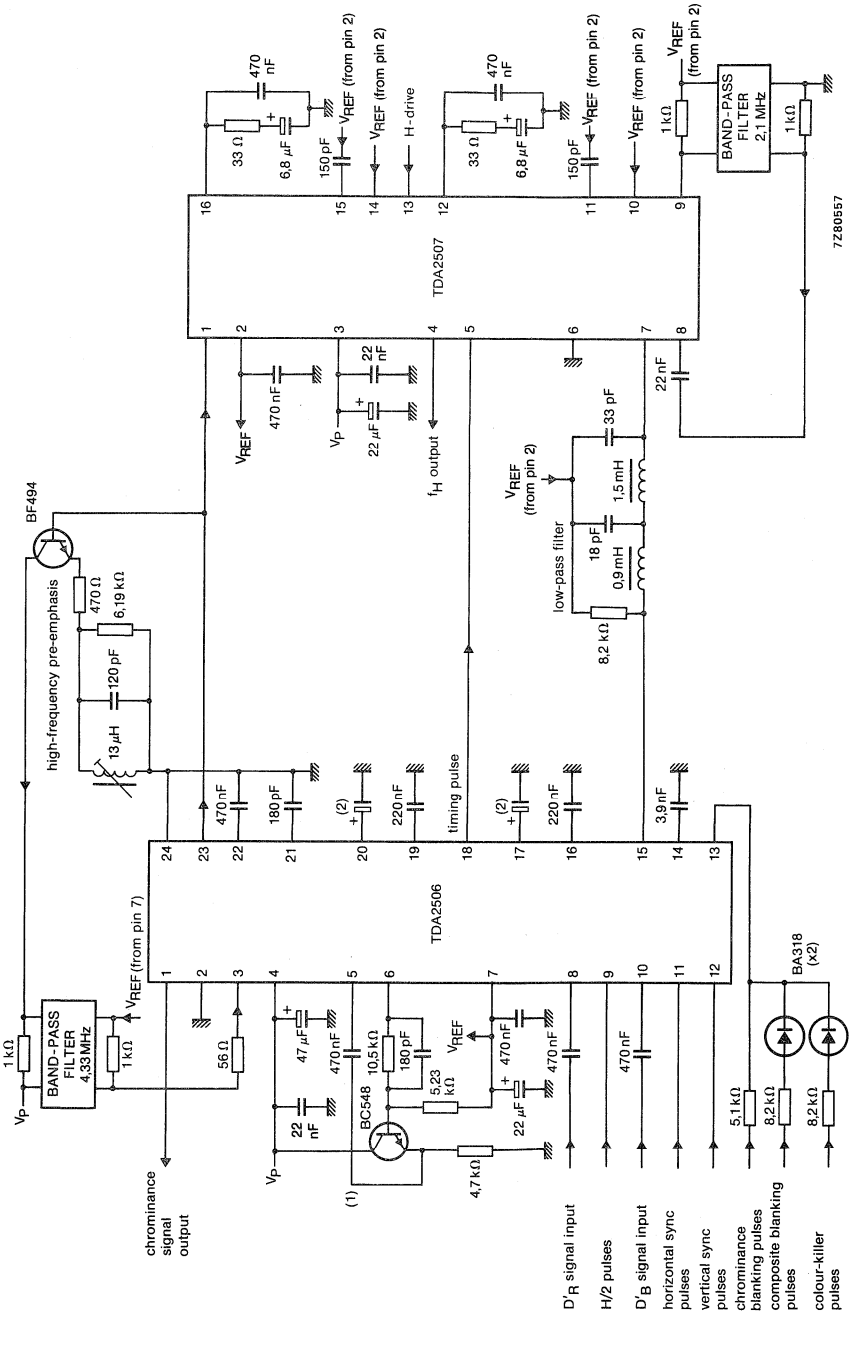
Values are valid for TDA2506 operating with TDA2507. Horizontal frequency (f_H) = 15 625 Hz.

parameter	symbol	min.	typ.	max.	unit
Centre frequency RED	f_{0R}	–	4 406,250 ± 2	–	kHz
Centre frequency BLUE	f_{0B}	–	4 250,000 ± 2	–	kHz
Ident. frequency RED *	f_{IdR}	–	4 756,250 ± 35	–	kHz
Ident. frequency BLUE *	f_{IdB}	–	3 900,000 ± 35	–	kHz
Minimum frequency RED **	$-f_R$	–	4 126,250 ± 10	–	kHz
Maximum frequency RED **	$+f_R$	–	4 686,250 ± 10	–	kHz
Minimum frequency BLUE **	$-f_B$	–	4 020,000 ± 10	–	kHz
Maximum frequency BLUE **	$+f_B$	–	4 480,000 ± 10	–	kHz

* The ident. frequencies are also the maximum and minimum output frequencies of the encoder.

** Values are valid for 75% colour bar saturation (EBU) (V_5 = ± 250 mV deviation from clamping level).

APPLICATION INFORMATION



(1) Signal amplitude for 75% colour bar (EBU) = 0,5 V (peak-to-peak value).
(2) For $V_P = 4{,}75$ to 5,3 V, $C_{17} = C_{20} = 0{,}68\ \mu F$; for $V_P > 5{,}3$ V, $C_{17} = C_{20} = 2{,}2\ \mu F$.

Fig. 6 Application using TDA2507 with PLL tuning: $V_P = 5$ V.

SECAM ENCODER

GENERAL DESCRIPTION

The TDA2506 converts colour-difference signals (D'_R and D'_B) into sequential, frequency modulated signals according to the SECAM system. The signals (D'_R) and (D'_B) are the colour difference signals before low-frequency pre-emphasis; $D'_R = -1,9$ (R-Y) and $D'_B = \pm 1,5$(B-Y). The circuit is intended for use in video cameras, games, recorders and players, PAL-SECAM transcoding circuits and SECAM test signal generators.

Synchronizing pulses required for operation of the TDA2506 may be obtained from a universal sync generator SAA1043 or other pulse generator. All pulses are to be active HIGH and are as follows:

Horizontal sync pulses to pin 11
Half-rate horizontal sync (H/2) pulses to pin 9
Vertical sync pulses to pin 12
Chrominance blanking pulses to pin 13 (may include colour-killer pulses)

Frequency modulation is performed in conjunction with modulator-controller TDA2507.

Features

- Chrominance processor
- Vertical identification signal generator
- Timing pulse output to TDA2507
- Sample and hold circuit for control signal from TDA2507
- No adjustments of external components required (except high-frequency pre-emphasis (bell filter) stage)

QUICK REFERENCE DATA

Supply voltage	V_{4-2}	typ.	5 V
Supply current	I_4	typ.	45 mA
Reference voltage	V_{7-2}, V_{22-24}	typ.	3,5 V
Operating ambient temperature range	T_{amb}		−25 to +70 °C
Storage temperature range	T_{stg}		−65 to +150 °C

PACKAGE OUTLINES

24-lead mini-pack ; plastic (SO-24 ; SOT-137A).

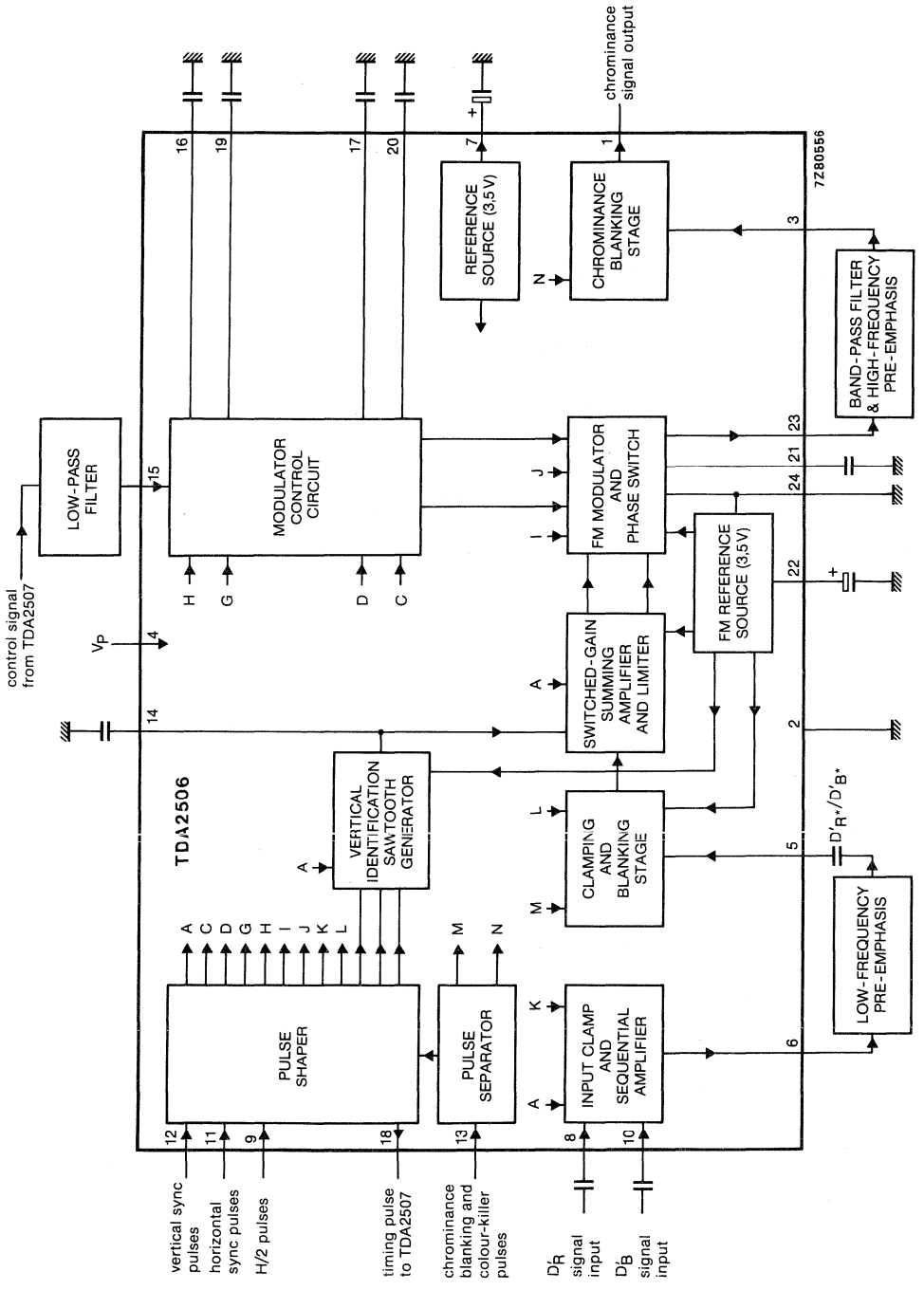


Fig. 1 Block diagram.

Pin functions

1. Chrominance signal output.
2. Ground.
3. Input to chrominance blanking stage from high-frequency pre-emphasis and band-pass filter.
4. Positive supply voltage.
5. Input to clamping and blanking stage from low-frequency pre-emphasis filter.
6. Output from sequential amplifier to low-frequency pre-emphasis filter.
7. Reference voltage output.
8. D'_R signal input.
9. H/2 pulse input (required only if specific phase sequencing is desired).
10. D'_B signal input.
11. Horizontal sync pulse input.
12. Vertical sync pulse input.
13. Chrominance blanking and colour-killer pulse input.
14. Capacitor for vertical identification sawtooth.
15. Control signal input from TDA2507 via low-pass filter.
16. 4 406,250 kHz frequency adjustment.
17. (R-Y) control.
18. Timing pulse output to TDA2507.
19. 4 250,000 kHz frequency adjustment.
20. (B-Y) control.
21. FM modulator tuning capacitor (fixed).
22. FM reference voltage output.
23. FM modulator output to high frequency pre-emphasis and band-pass filter.
24. Ground connection for FM modulator.

FUNCTIONAL DESCRIPTION

Input clamp and sequential amplifier

This circuit clamps the zero levels of the D'_R and D'_B input signals (pins 8 and 10) to the reference voltage from pin 7. The input signals are switched into the amplifier sequentially by an internally delayed H/2 waveform. The amplifier output at pin 6 is D'_R when the delayed H/2 waveform is HIGH and D'_B when it is LOW. The stage gain is 1,5.

Clamping and blanking stage

After external low-frequency pre-emphasis, the sequential $D'_R{}^*$ and $D'_B{}^*$ signals are returned to the IC at pin 5. The signal amplitude at pin 5 is typically 0,5 V (peak-to-peak value) for 75% colour bar (EBU). Black levels are clamped to the FM reference voltage (pin 22). Blanking takes place during the chrominance blanking pulse and, if required, during the video blanking and/or colour killing pulses.

FUNCTIONAL DESCRIPTION (continued)

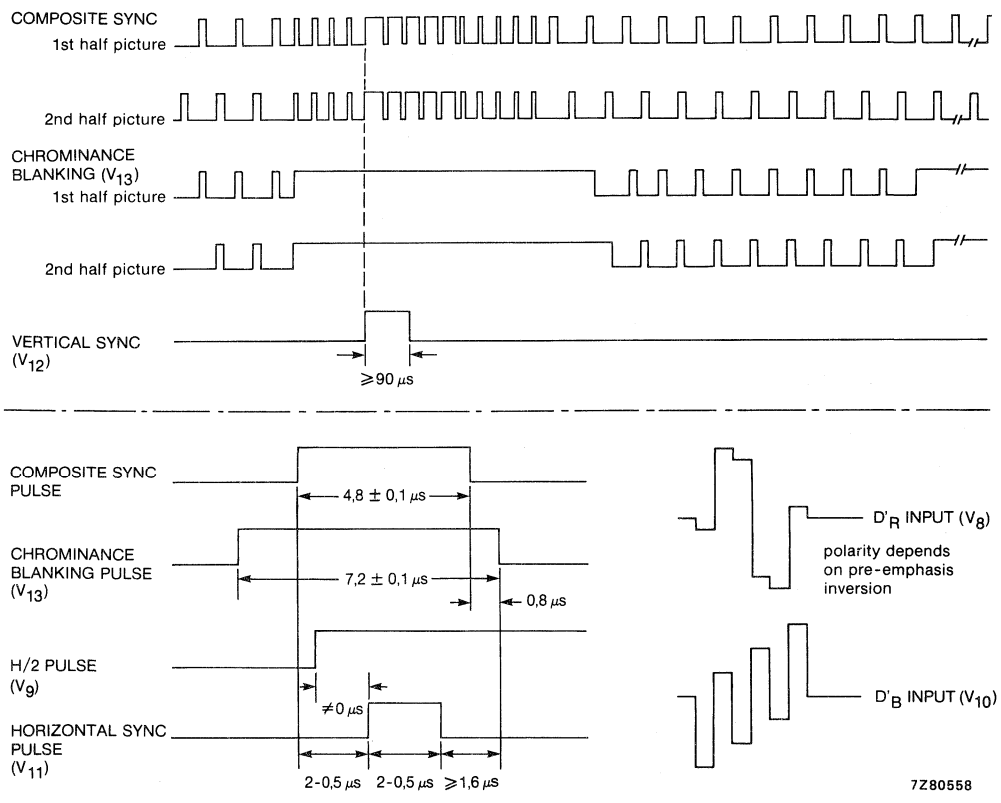


Fig. 2 Survey of input signals in relation to composite sync.

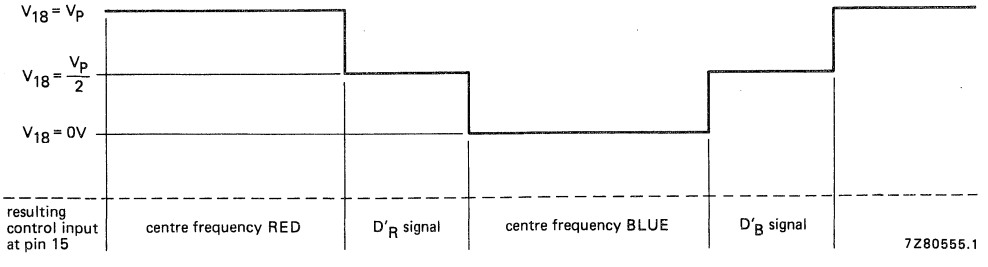


Fig. 3 Timing pulse output (pin 18) and resulting control input (pin 15).

Switched-gain summing amplifier and limiter

Inputs into the summing amplifier are the sequential D'_R* and D'_B* signals, the vertical identification sawtooth waveform and reference d.c. levels. The gain of the amplifier is switched by the internally delayed H/2 waveform to give the correct input amplitudes for the FM modulator (D'_R* gain = 280/230 x D'_B* gain). An offset is also introduced between the black levels of the D'_R* and D'_B* signals which corresponds to the upper and lower thresholds of the limiter.

FM modulator and phase switch

The FM modulator provides accurate FM modulation which follows the amplitude envelopes of the sequential D'_R* and D'_B* waveforms. The centre frequencies of 4 406,250 kHz for the D'_R* signal and 4 250,000 kHz for the D'_B* signal are controlled by d.c. levels from the sample and hold circuit (which in turn are controlled by the TDA2507). The upper and lower frequency limits are 4 756,250 ± 35 kHz and 3 900,000 ± 35 kHz.

Reference d.c. levels are switched within the FM modulator to define the starting phase of the modulator output (pin 23) at the initiation of each horizontal and vertical scan. The starting phase sequence is as follows:

vertical scan (frame to frame) 0^o, 180^o, 0^o, 180^o, repeating;

horizontal scan (line to line) 0^o, 0^o, 180^o, 0^o, 0^o, 180^o, repeating.

Chrominance blanking stage

The frequency modulated colour difference signals are passed via high-frequency pre-emphasis and band-pass filters to the chrominance blanking input at pin 3. The d.c. level of this input should be equal to the reference voltage at pin 7. Blanking occurs during the chrominance blanking pulse. The stage gain is 1,75.

Vertical identification sawtooth generator

Vertical sync, horizontal sync and chrominance blanking pulses are used to determine vertical identification (see Fig. 4). The vertical identification sawtooth generator is driven in opposite directions for identification signals IdR and IdB; the capacitor for the generator is connected at pin 14. If no vertical identification is required, pin 14 should be connected to the FM reference voltage at pin 22.

Pulse shaper

This stage developes all pulses that are required within the TDA2506 and also the timing pulses required for the modulator controller TDA2507 (see Fig. 3). Internal H/2 pulses are generated by a flip-flop working from the horizontal sync input (pin 11), this makes the H/2 input at pin 9 necessary only if it is required to lock the modulator into a specific phase sequence. If the H/2 input is not required, pin 9 should be connected to ground. A pulse separator at the chrominance blanking/colour-killer input (pin 13) allows this input to be used for blanking the sequential D'_R*/D'_B* signal.

Sample and hold circuit

This circuit provides reference voltages to the FM modulator which set the centre modulation frequencies for the sequential D'_R* and D'_B* signals. The reference voltage levels are supplied to pin 15 from the TDA2507 in a sequence that is time-related to D'_R*/D'_B* switching. The levels are sampled and then held for D'_R* using capacitors at pins 16 and 17, and for D'_B* using capacitors at pins 19 and 20.

FUNCTIONAL DESCRIPTION (continued)

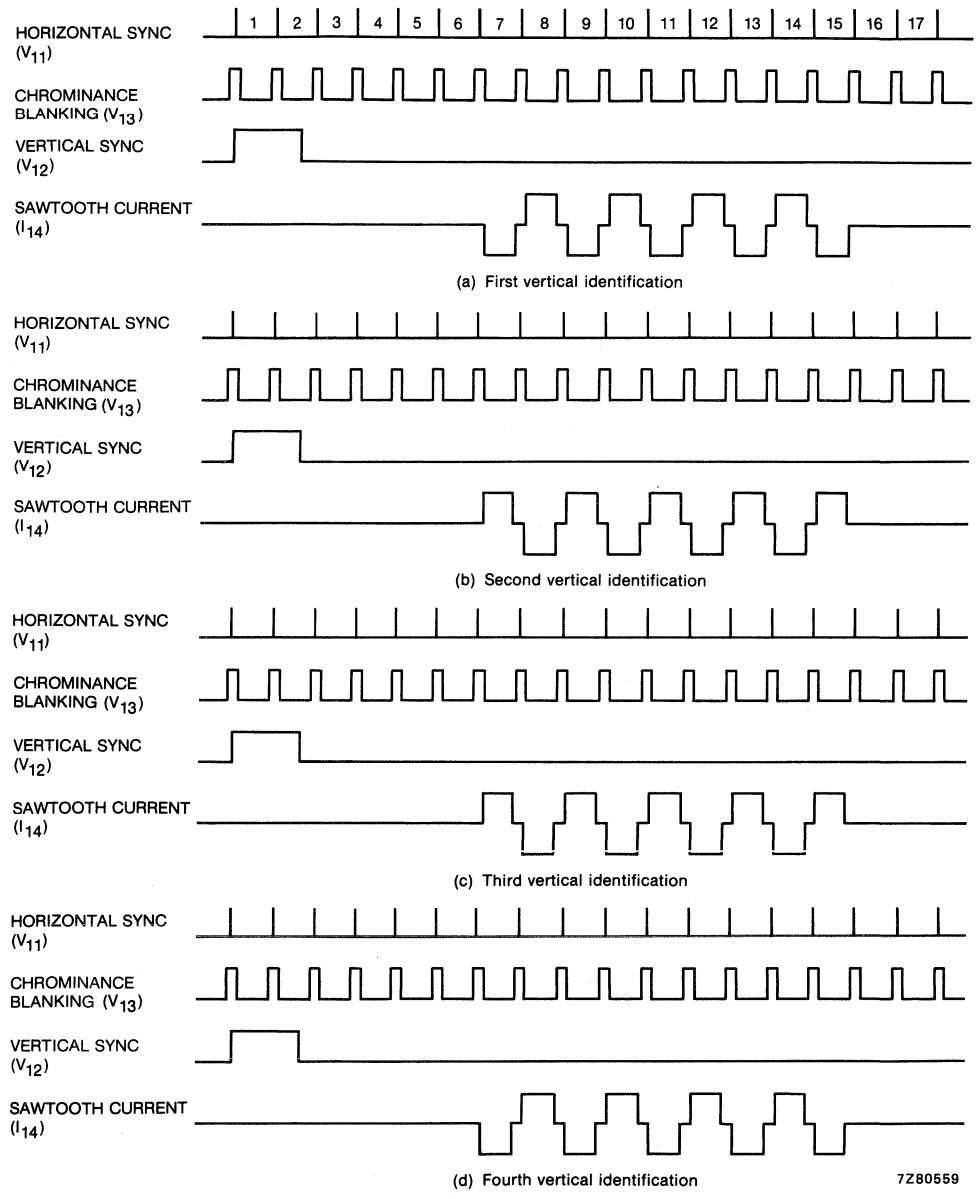


Fig. 4 Vertical identification generation.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating system IEC 134

Supply voltage	V_{4-1}	max. 13,2 V
Total power dissipation	P_{tot}	see Fig. 5
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−65 to +150 °C

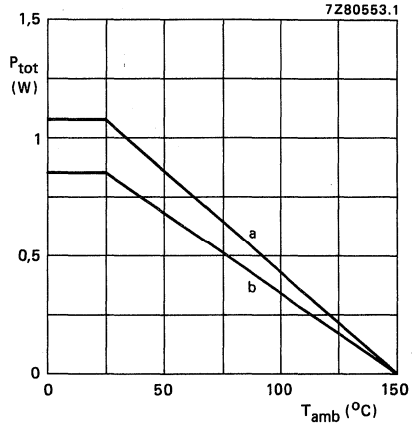


Fig. 5 Power derating curve.

a = device mounted on a ceramic substrate.
b = device mounted on a printed circuit board.

CHARACTERISTICS

$V_p = V_{4-2} = 5$ V; $T_{amb} = 25$ °C; all voltages are with reference to ground (pins 2 and 24); all currents stated are positive into the IC; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage (pin 4)	$V_p = V_{4-2}$	4,75	5	7	V
Supply current	$I_p = I_4$	30	45	60	mA
Reference voltage (pin 7)	V_{7-2}	3,35	3,5	3,65	V
Reference voltage (pin 22)	V_{22-24}	3,35	3,5	3,65	V
Pulse shaper (pins 9,11 and 12, emitter follower inputs; pin 18, collector output)					
Bias current (pin 9,11,12)	I_9, I_{11}, I_{12}	–	–	10	μA
Input resistance (pin 9,11,12)	R_9, R_{11}, R_{12}	200	–	–	kΩ
Input pulse amplitude (pin 9,11,12)	V_9, V_{11}, V_{12}	2	–	–	V
Timing pulse output (pin 18) high level	V_{18}	4,7	–	–	V
intermediate ($V_p/2$) level	V_{18}	2,3	–	2,7	V
low level	V_{18}	–	–	0,3	V
Pulse separator (pin 13, emitter follower)					
Input resistance	R_{13}	100	–	–	kΩ
Chrominance blanking pulse amplitude	V_{13}	3,6	–	–	V
D'_R*/D'_B* blanking pulse amplitude (colour killing)	V_{13}	1,7	1,8	1,9	V
Vertical identification sawtooth generator (pin 14)					
Voltage clamping level	V_{14}	V_{22}–7 mV	V_{22}	V_{22}+7 mV	V
Ramp current (occurs in lines 7 to 15 after vertical sync)	$\pm I_{14}$	50	70	85	μA
Maximum voltage level	V_{14}	V_{22}+0,6	V_{22}+0,7	V_{22}+0,8	V
Minimum voltage level	V_{14}	V_{22}–0,8	V_{22}–0,7	V_{22}–0,6	V
Voltage level during line blanking	V_{14}	V_{22}–7 mV	V_{22}	V_{22}+7 mV	V
Inputs D'_R*, D'_B* (pins 8 and 10)					
Signal level during clamping ($I_8, I_{10} = \pm 50$ μA)	V_8, V_{10}	V_7–20 mV	V_7	V_7+20 mV	V
Input bias current	I_8, I_{10}	–	–	1,5	μA

parameter	symbol	min.	typ.	max.	unit
Sequential amplifier output (pin 6)					
(Pins 8 and 10 a.c. coupled to fixed d.c. voltage)					
D.C. output	V_6	1,6	$\frac{V_7 - 10\ mV}{2}$	1,85	V
Output resistance	R_6	–	12	16	Ω
Amplifier voltage gain (pin 8 or 10 to pin 6)	$G_{8,10-6}$	1,46	1,5	1,54	
Clamping and blanking stage (pin 5)					
Input voltage (clamped; $I_5 = \pm 50\ \mu A$)	V_5	$V_{22} - 10\ mV$	V_{22}	$V_{22} + 10\ mV$	V
Input bias current	I_5	–	–	1,0	μA
Modulator control circuit (pin 15, buffer amplifier non-inverting input)					
Bias current	I_{15}	–	–	1,25	μA
Permitted input signal d.c. levels	V_{15}	2	–	4,3	V
FM modulator output (pin 23, emitter follower)					
Output resistance	R_{23}	–	50	70	Ω
High d.c. output level at $V_{21} = 4\ V$	V_{23}	$V_{22} - 0,85$	–	$V_{22} - 0,7$	V
Output signal amplitude	V_{23}	0,9	1,0	1,1	V

CHARACTERISTICS (Continued)

parameter	symbol	min.	typ.	max.	unit
Chrominance blanking stage (pin 3, emitter follower input; pin 1, amplifier output)					
Input current	I_3	–	–	15	μA
Input resistance	R_3	300	–	–	kΩ
Required d.c. level of input signal	V_3	–	V_7	–	V
Output resistance	R_1	–	–	5	Ω
Temperature coefficient of output d.c. level	TC	–	1,8	—	mV/K
Amplifier gain	G_{3-1}	1,70	1,75	1,80	
Output d.c. level during blanking(V_{13} = HIGH)	V_1	V_7–0,76	V_7–0,70	V_7–0,60	V
Output d.c. level unblanked ($V_3 = V_7$; V_{13} = LOW)	V_1	V_7–0,76	V_7–0,70	V_7–0,60	V

A.C. CHARACTERISTICS

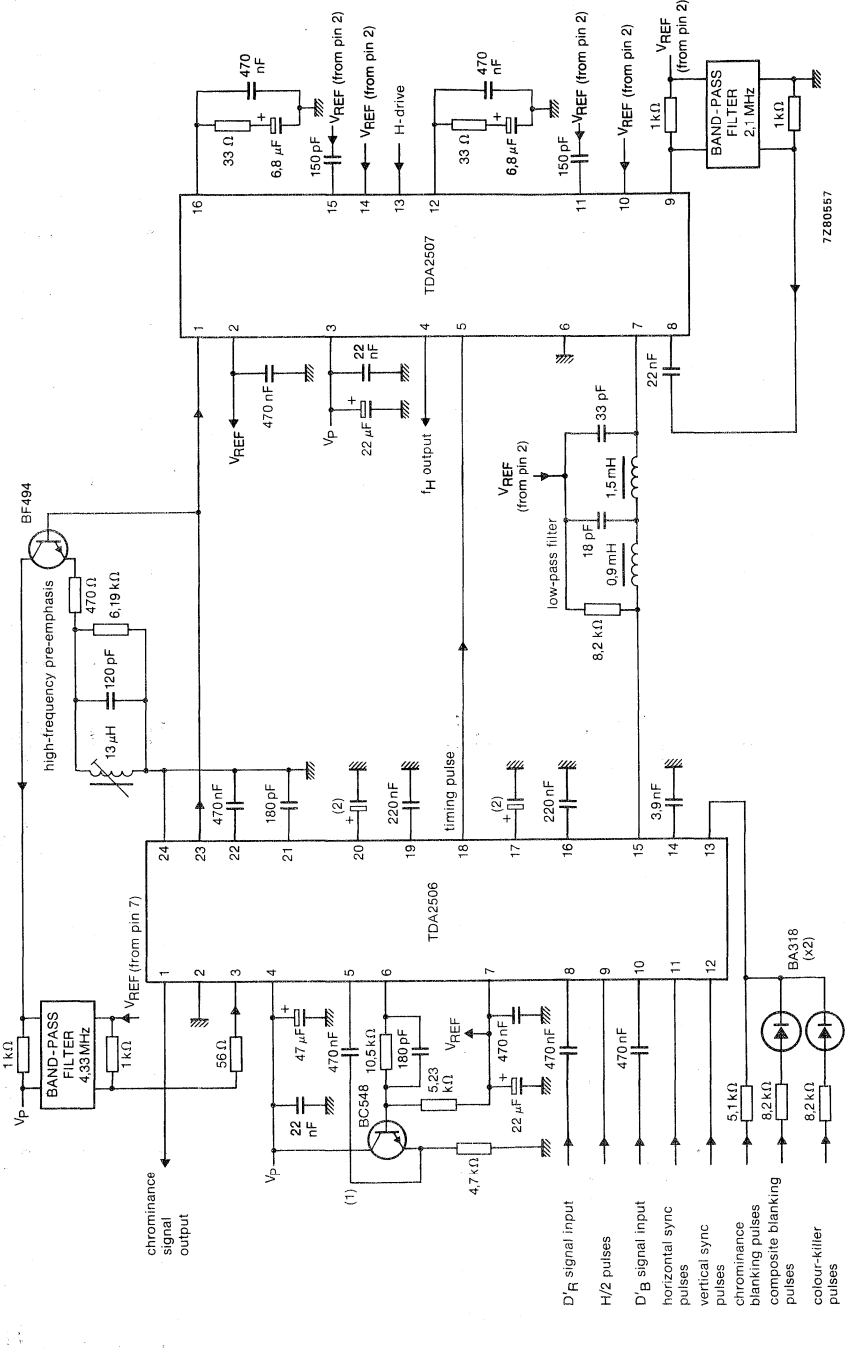
Values are valid for TDA2506 operating with TDA2507. Horizontal frequency (f_H) = 15 625 Hz.

parameter	symbol	min.	typ.	max.	unit
Centre frequency RED	f_{0R}	–	4 406,250 ± 2	–	kHz
Centre frequency BLUE	f_{0B}	–	4 250,000 ± 2	–	kHz
Ident. frequency RED *	f_{IdR}	–	4 756,250 ± 35	–	kHz
Ident. frequency BLUE *	f_{IdB}	–	3 900,000 ± 35	–	kHz
Minimum frequency RED **	$-f_R$	–	4 126,250 ± 10	–	kHz
Maximum frequency RED **	$+f_R$	–	4 686,250 ± 10	–	kHz
Minimum frequency BLUE **	$-f_B$	–	4 020,000 ± 10	–	kHz
Maximum frequency BLUE **	$+f_B$	–	4 480,000 ± 10	–	kHz

* The ident. frequencies are also the maximum and minimum output frequencies of the encoder.

** Values are valid for 75% colour bar saturation (EBU) (V_5 = ± 250 mV deviation from clamping level).

APPLICATION INFORMATION



(1) Signal amplitude for 75% colour bar (EBU) = 0,5 V (peak-to-peak value).
(2) For $V_P = 4{,}75$ to 5,3 V, $C_{17} = C_{20} = 0{,}68\ \mu F$; for $V_P > 5{,}3$ V, $C_{17} = C_{20} = 2{,}2\ \mu F$.

Fig. 6 Application using TDA2507 with PLL tuning: $V_P = 5$ V.

FM MODULATOR CONTROLLER

GENERAL DESCRIPTION

The TDA2507 accepts FM signals that are sequentially modulated by two alternating subcarrier frequencies (SECAM signals) and provides sequential DC output levels to control the FM modulator.

The IC is intended for use with the SECAM encoder TDA2506 but can be adapted for other applications. Timing reference pulses from the modulator are required.

Two frequency reference phase-lock loops are contained within the IC; one for 4.40625 MHz, and one for 4.250 MHz. Other frequencies can be accomplished by using external reference sources.

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (pin 3)		$V_P = V_{3-6}$	4.75	5.0	7.0	V
Supply current	V_P = 5 V; both PLL circuits on	I_3	–	40	–	mA
Reference voltage		V_{2-6}	3.38	3.5	3.6	V
Storage temperature range		T_{stg}	−65	–	+150	°C
Operating ambient temperature range		T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

TDA2507 : 16-lead DIL; plastic (with internal heat spreader) (SOT38).
TDA2507T: 16-lead mini-pack; plastic (SO16L; SOT162A).

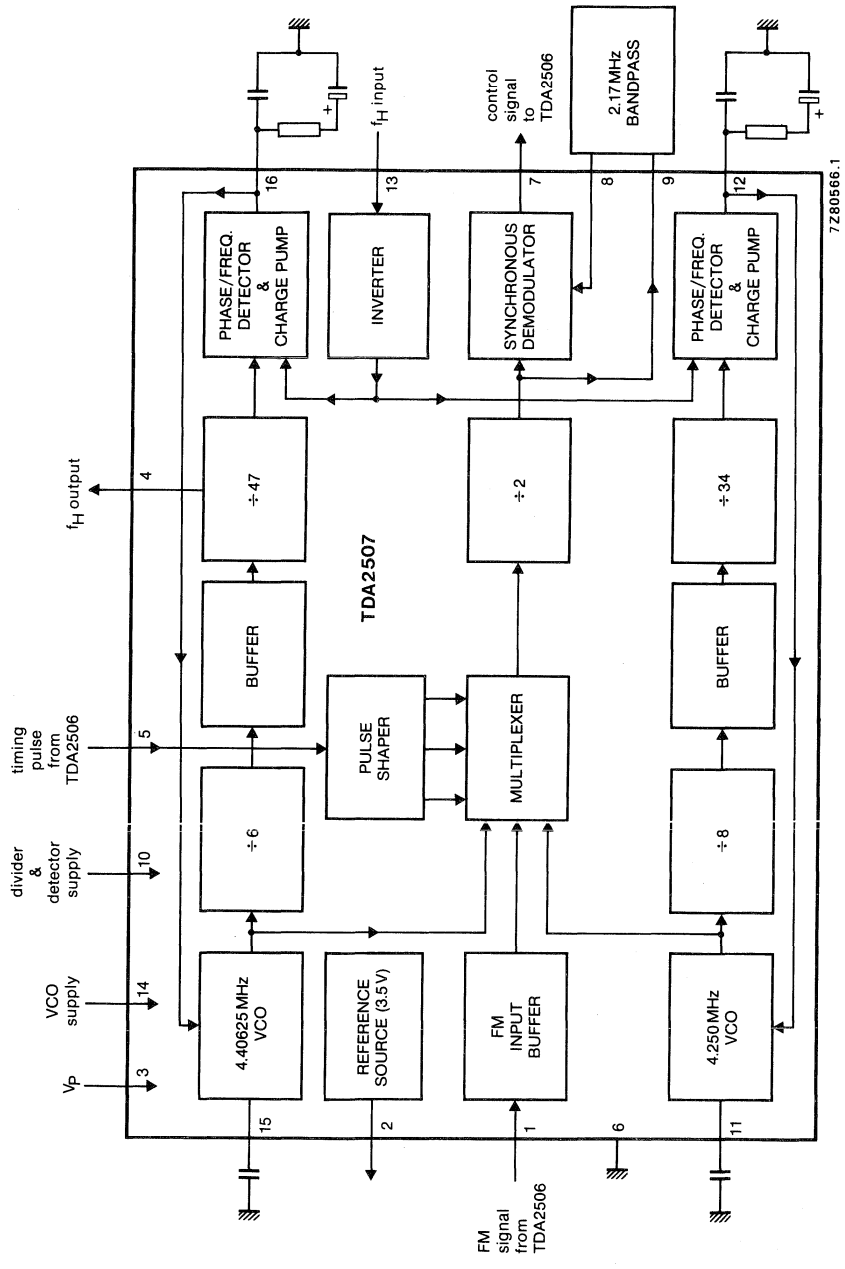


Fig.1 Block diagram.

PINNING

Pin functions

pin	description
1	FM signal input (from TDA2506)
2	Reference voltage output
3	Positive supply voltage
4	Horizontal sync output (f_H = 4 406.250/282 = 15.625 kHz)
5	Timing pulse input (from TDA2506)
6	Ground
7	Control signal output to TDA2506 via low-pass filter
8	Input to synchronous demodulator from band-pass filter
9	Output to band-pass filter
10	Supply voltage for the divider stages and phase/frequency detectors of the two phase-lock loops (PLL)
11	Tuning capacitor for the 4.250 MHz reference oscillator
12	Filter for the phase/frequency detector of the 4.250 MHz phase-lock loop
13	Horizontal sync input (f_H)
14	Supply voltage for the two reference oscillators
15	Tuning capacitor for the 4.40625 MHz reference oscillator
16	Filter for the phase/frequency detector of the 4.40625 MHz phase-lock loop.

FUNCTIONAL DESCRIPTION

Phase-lock loops

The two phase-lock loops each comprise a voltage-controlled reference oscillator, two frequency divider stages and a phase/frequency detector circuit. The loops are closed by charge pumping the reference oscillators from the phase/frequency detector outputs. The centre frequencies of the loops are set by external capacitors at pin 15 (4.40625 MHz) and pin 11 (4.250 MHz). The divider stages which follow the reference oscillators reduce the frequencies of both the loops to 15.625 kHz (f_H) at their respective inputs to the phase/frequency detectors. The reference signals to both phase/frequency detectors are obtained from the horizontal sync input at pin 13.

The divider and phase/frequency detector circuits can be switched off by connecting pin 10 to ground. This leaves only the VCO of each PLL in circuit and allows external signals to be injected at pins 15 and 11, or crystals to be used for tuning the oscillators.

The accuracy of crystal tuning using only one crystal can be obtained by connecting pins 10, 14 and 16 to the reference voltage at pin 2 and connecting a 4.40625 MHz crystal to pin 15. The 4.250 MHz PLL will follow the crystal-derived f_H reference from pin 4 via pin 13 and its phase/frequency detector.

Multiplexer and pulse shaper

The multiplexer receives the 4.40625 and 4.250 MHz reference frequencies from the two VCOs and the FM signals $D'_R{}^*$ and $D'_B{}^*$ from the TDA2506 modulator. The signals are gated one at a time to the multiplexer output in a sequence determined by the timing pulses from TDA2506. The levels of the timing pulses (pin 5) are used in the pulse shaper to generate enable pulses for the multiplexer (see Figs 2 and 3). The multiplexer output sequence is as follows:

4.40625 MHz (2 lines); $D'_R{}^*$ FM signal (1 line); 4.250 MHz (2 lines); $D'_B{}^*$ FM signal (1 line); repeating. The selection of $D'_R{}^*$ or $D'_B{}^*$ FM signal is a feature of the timing of the input at pin 5.

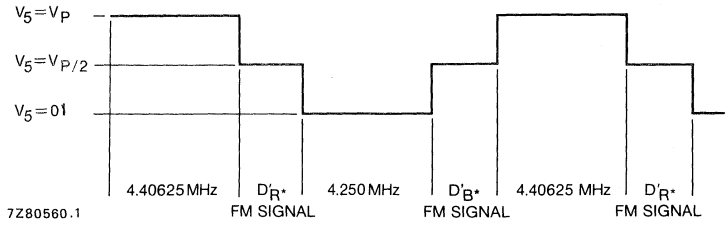


Fig.2 Timing pulse waveform for multiplexer output sequence.

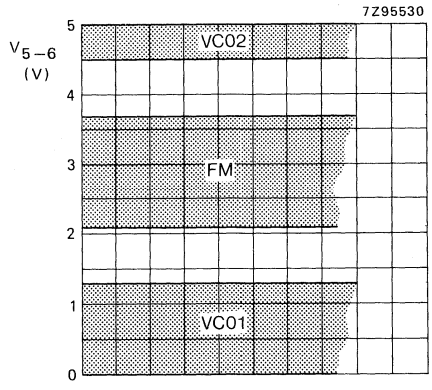


Fig.3 Switching levels of the timing pulse at pin 5.

Divide-by-two stage and synchronous demodulator

The divide-by-two stage halves the frequencies present in the multiplexer output and equalizes the amplitude and pulse shapes of the sequential signals.

Demodulation of the multiplexed signal is performed by filtering the signal via a 2.17 MHz band-pass filter (between pins 8 and 9) and using this filtered signal as a synchronous switch for the main signal. The DC level of the signal from pin 9 is referred externally to the reference voltage from pin 2. An external low-pass filter is required for the output signal from pin 7.

RATINGS

Limiting values in accordance with the Absolute Maximum Rating system IEC 134

parameter	symbol	min.	max.	unit
Supply voltage (pin 3)	V_P	–	13.2	V
Total power dissipation	P_{tot}	see Fig.4		W
Operating ambient temperature range	T_{amb}	−25	+70	°C
Storage temperature range	T_{stg}	−65	+150	°C

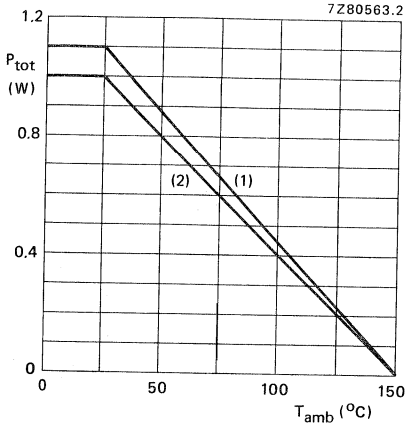
CHARACTERISTICS

$V_P = V_{3-6} = 5$ V; $T_{amb} = 25$ °C; all voltages are with reference to ground; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supplies						
Supply voltage (pin 3)		V_P	4.75	5.0	7.0	V
Supply current	$V_{14} = V_{10} = V_2$	I_P	–	35	–	mA
Supply current	$V_{14} = V_2$	I_P	–	20	–	mA
Reference voltage (pin 2)		V_{2-6}	3.38	3.5	3.6	V
Phase-lock loops						
DC voltage output level						
pin 11		V_{11-6}	2.4	2.6	2.8	V
pin 15		V_{15-6}	2.4	2.6	2.8	V
Amplitude of oscillation (peak-to-peak value)						
pin 11		$V_{11(p-p)}$	–	130	–	mV
pin 15		$V_{15(p-p)}$	–	130	–	mV
Input current	see Fig.5					
pin 11	$V_{12-6} = 1.5$ V	I_{11}	–	130	–	μA
pin 15	$V_{16-6} = 1.5$ V	I_{11}	–	130	–	μA
Limiting values for VCO control voltages						
pin 12		V_{12}	0.8	–	1.9	V
pin 16		V_{16}	0.8	–	1.9	V
Output resistance at pin 4	V_4 = HIGH	R_4	5.1	6.8	8.5	kΩ
Input resistance at pin 13		R_{13}	200	–	–	kΩ
Amplitude of f_H pulse required at pin 13	note 1	V_{13}	2	–	–	V
FM input buffer (pin 1)						
Input resistance		R_1	180	–	–	kΩ
Switching level of FM input		V_1	2.2	2.3	2.4	V
Required input amplitude		V_1	0.5	–	2.0	V
Pulse shaper input (pin 5)						
Input resistance		R_5	200	–	–	kΩ
Demodulator						
Sink current at pin 9 into divide-by-two circuit	V_9 = LOW	I_9	0.6	0.9	1.2	mA
Demodulator input bias voltage at pin 8		V_8	1.60	1.68	1.76	V
Demodulator output current from pin 7	see Fig.6					
output current at A		$-I_7$	0.6	0.9	1.2	mA
output current at B		I_7	1.2	0.9	0.6	mA

Note to the characteristics

1. Duty factor and timing not important.



(1) Device mounted on a ceramic substrate
(2) Device mounted on a printed-circuit board

Fig.4 Power derating curve.

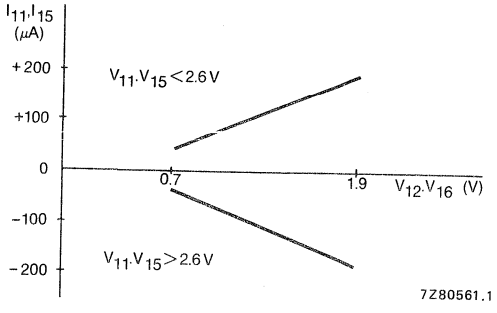


Fig.5 Current input to pins 11 and 15 as a function of voltage at pins 12 and 16 (typical values).

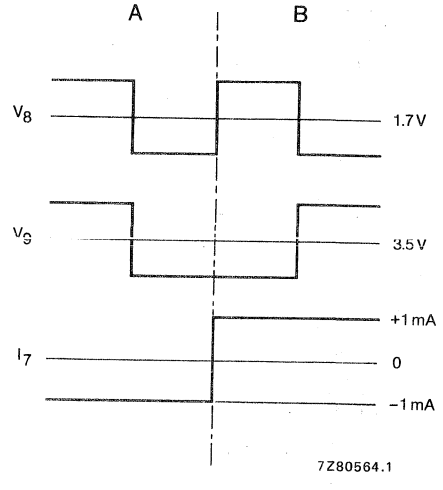


Fig.6 Demodulator output current from pin 7 (typical values).

APPLICATION INFORMATION

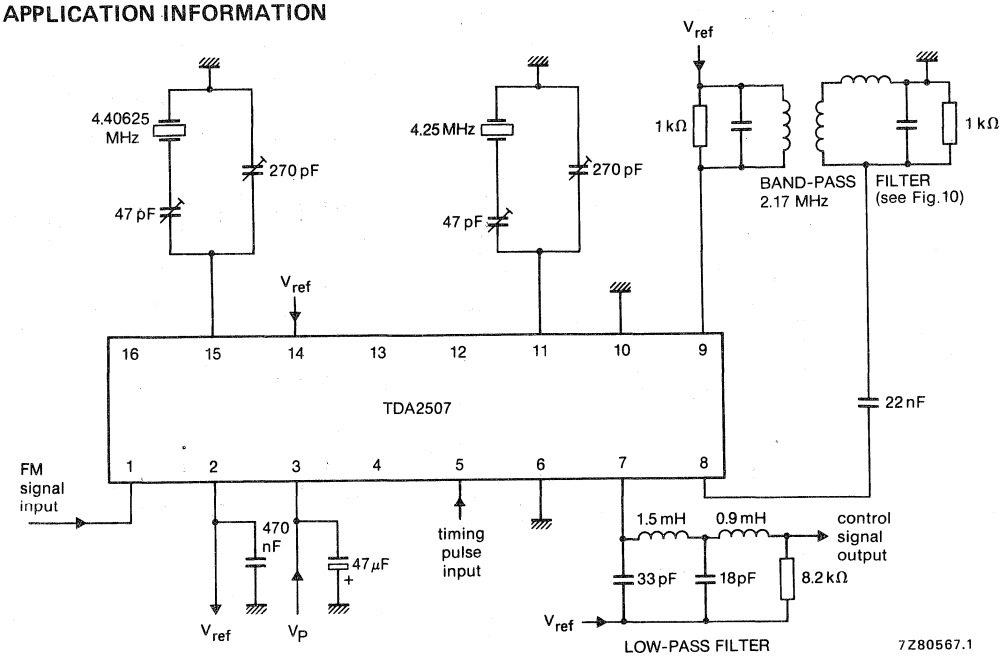


Fig.7 Application diagram using two crystals for tuning; V_P = 5 V.

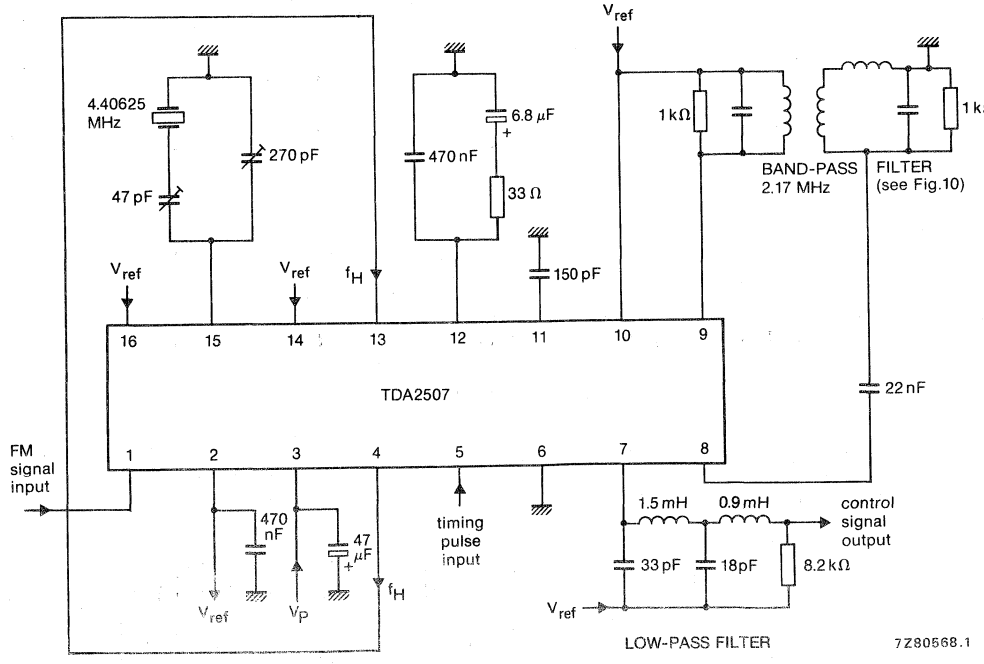


Fig.8 Application diagram using single crystal tuning; V_P = 5 V.

APPLICATION INFORMATION (continued)

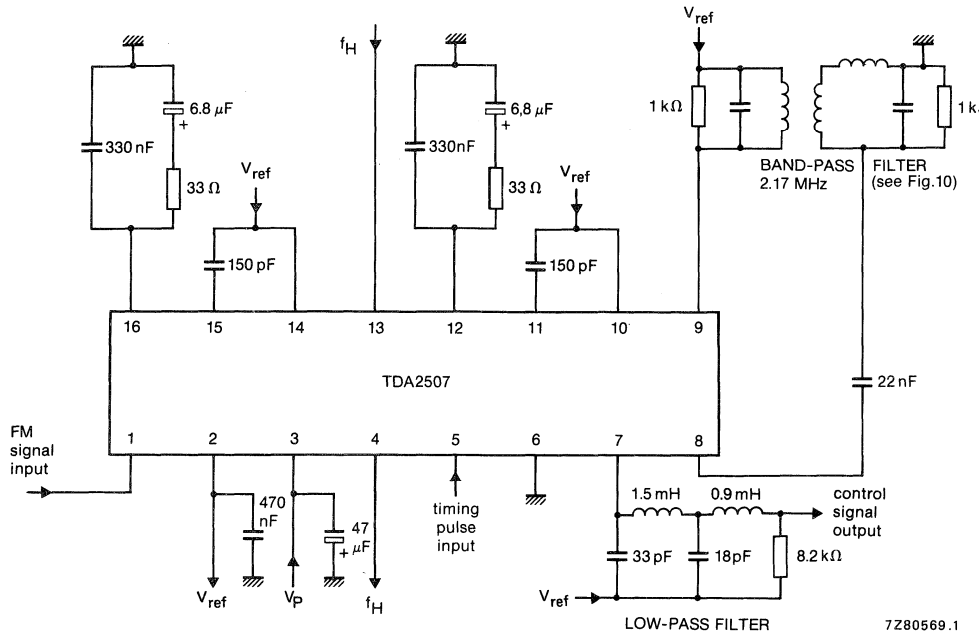


Fig.9 Application diagram using PLL tuning; V_P = 5 V.

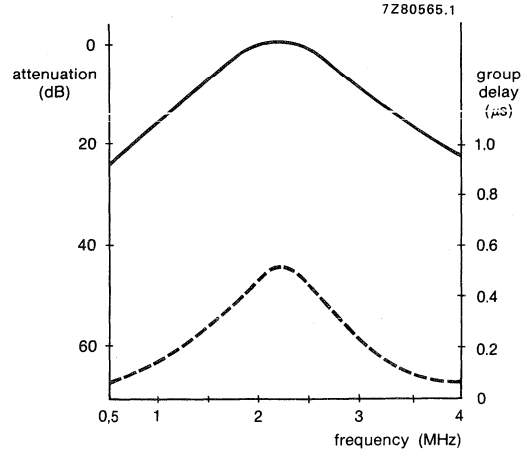


Fig.10 Typical response of 2.17 MHz band-pass filter.

WHITE PROCESSING ENCODER

GENERAL DESCRIPTION

The TDA4303 is an integrated circuit that operates in conjunction with the PAL-NTSC encoder (TDA2501) to form the colour encoder part of a television camera. This circuit can also operate in conjunction with the SECAM encoder (TDA2506) and the FM modulator controller (TDA2507) for the SECAM system.

Features

Processing part

- Four input clamping circuits to determine the black levels
- Three $1/\gamma$ correction circuits
- Four blanking circuits
- Four white clipping circuits
- Colour matrix; that delivers
  - U (with respect to colour difference signal D'_B)
  - V (with respect to colour difference signal D'_R)
  - Y and the W signal

CVBS part

- Chrominance, luminance and synchronized summation circuit
- Contour amplifier
- A black and a white clipping circuit in the output stage
- Output stage with the capability to drive a 75 Ω coaxial cable system

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 13)	$V_P = V_{13-27}$	4,75	5,0	5,25	V
Supply current (pin 13)	I_P	–	65	–	mA
Storage temperature range	T_{stg}	−25	–	+ 150	°C
Operating ambient temperature range	T_{amb}	−20	–	+ 70	°C

PACKAGE OUTLINES

TDA4303: 28-lead DIL; plastic with internal heat spreader (SOT117).
TDA4303T: 28-lead mini-pack; plastic (SO28; SOT136A).

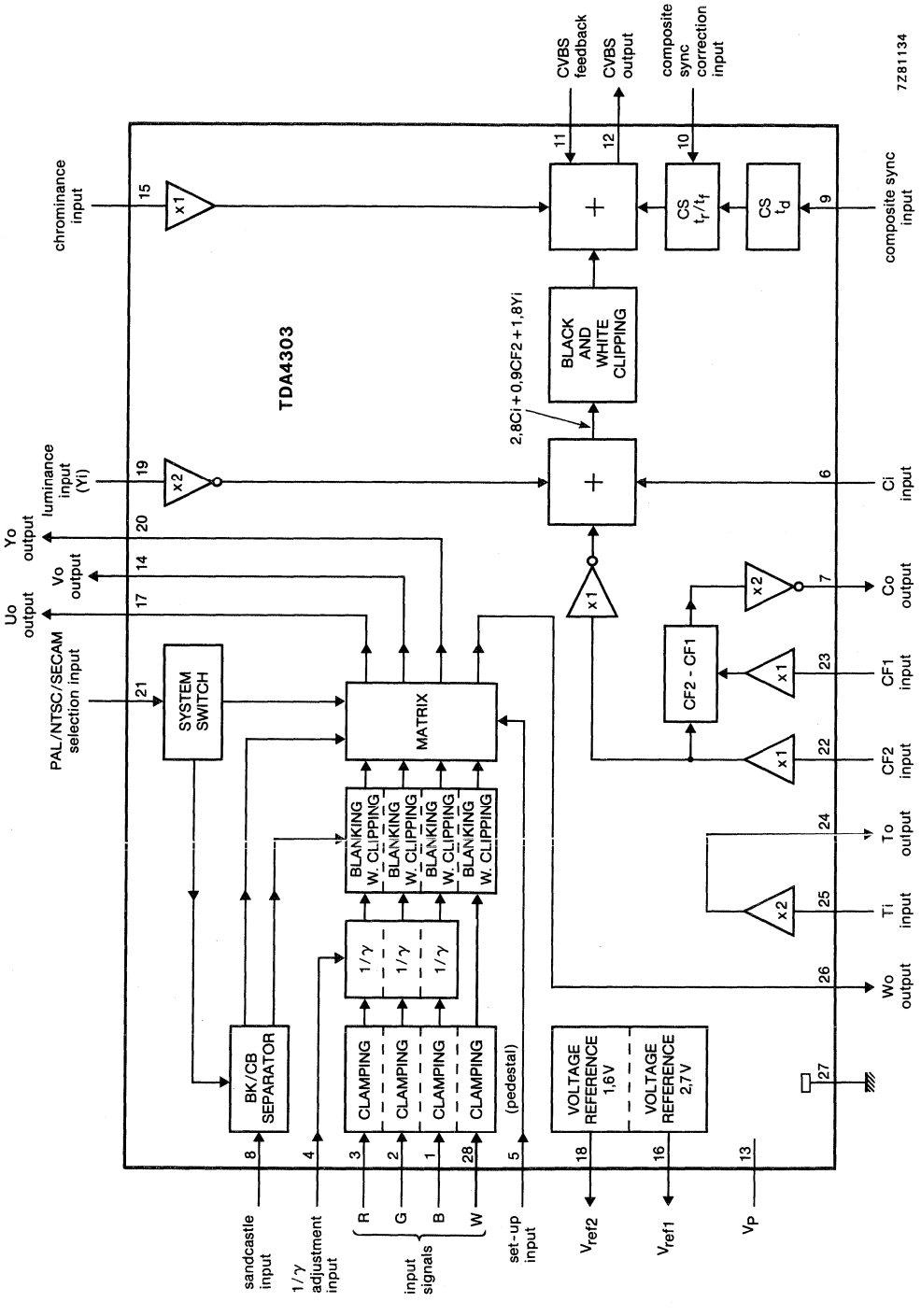


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 13)	V_P	–	12	V
Total power dissipation				
SO package*	P_{tot}	–	730	mW
DIL package	P_{tot}	–	1000	mW
Operating ambient temperature range	T_{amb}	–20	+ 70	°C
Storage temperature range	T_{stg}	–25	+ 150	°C

DEVELOPMENT DATA

* Mounted on a printed-circuit board.

CHARACTERISTICS

$V_P = V_{13-27} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 13)	V_P	4.75	5	5.25	V
Supply current (pin 13) (75 Ω resistor to CVBS output)	I_P	–	65	–	mA
PROCESSING PART					
Input signals RGB and W R (pin 3); G (pin 2); B (pin 1); W (pin 28) (peak-to-peak value)	$V_{n-27(p-p)}$	–	1.0	1.3	V
Uo output signal (pin 17; peak value) at $V_{1-27(p-p)} = 1$ V	$V_{17-27(M)}$	0.68	0.72	0.75	V
Vo output signal (pin 14; peak value) for PAL and NTSC at $V_{3-27(p-p)} = 1$ V	$V_{14-27(M)}$	0.95	1.0	1.05	V
Vo (D'_R) output signal (pin 14; peak value) for SECAM at $V_{3-27(p-p)} = 1$ V	$V_{14-27(M)}$	0.68	0.72	0.75	V
Yo output (pin 20; peak value) at $V_{3, 2, 1-27(p-p)} = 1$ V and $V_{28-27(p-p)} = 0$ V	$V_{20-27(M)}$	0.95	1.0	1.05	V
Wo output (pin 26; peak value) at $V_{28-27(p-p)} = 1$ V	$V_{26-27(P)}$	0.95	1.0	1.05	V
$1/\gamma$ tracking between Uo, Vo and Yo outputs		–	1	2	%
$1/\gamma$ correction of Uo, Vo and Yo*		0.50	0.55	0.65	
Ratio $\frac{Yo}{Wo}$ at $V_{28-27(p-p)} = 1$ V		0.95	1.00	1.05	
Set-up Yo output at $V_{pedestal} = V_{ref2} - 0.1$ V		–	0.1	–	V
White clipping Uo, Yo and Wo outputs with respect to 1 V(p-p)		–	120	–	%

* 2.2 kΩ (± 5%) load resistor connected between $1/\gamma$ control input (pin 4) and ground (pin 27).

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Burst amplitude during PAL					
(system switch V_{21-27} = 5 V)					
Uo output (with respect to black level) (peak-to-peak value)	$V_{17-27(p-p)}$	−233	−246	−258	mV
Vo output (with respect to black level) (peak-to-peak value)	$V_{14-27(p-p)}$	233	246	258	mV
Ratio $\frac{\text{Burst Uo}}{\text{Burst Vo}}$	$\frac{V_{17-27}}{V_{14-27}}$	0.965	1.0	1.035	
Burst amplitude during NTSC					
(system switch V_{21-27} = 0 V)					
Uo output (with respect to black level) (peak-to-peak value)	$V_{17-27(p-p)}$	−330	−350	−370	mV
DC output voltage levels					
Uo and Vo outputs	$V_{17,\,14-27}$	2.3	2.5	2.7	V
Yo and Wo outputs	$V_{20,\,26-27}$	–	1.6	–	V
Black level decay of Vo, Uo, Yo and Wo outputs (during video scanning)	V_{n-27}	–	–	6	mV
Reference voltage V_{ref2}	V_{18-27}	1.4	1.6	1.8	V
Reference voltage V_{ref1}	V_{16-27}	2.5	2.7	2.9	V
Power supply rejection ratio at Vo, Uo, Yo and Wo outputs (1 kHz)	R/R	–	*	–	dB
System switch (pin 21)					
PAL system ON	V_{21-27}	3.8	–	–	V
SECAM system ON	V_{21-27}	1.4	–	3.1	V
NTSC system ON	V_{21-27}	–	–	1.0	V
Sandcastle input (pin 8)					
Threshold burst key	V_{8-27}	2.5	3.75	V_P	V
Input current at V_{8-27} = 5 V	I_8	–	500	–	μA
Threshold composite blanking	V_{8-27}	–	1.25	2.5	V
Input current at V_{8-27} = 2.5 V	I_8	–	5	–	μA
Input leakage current at V_{8-27} = 0 V	$\pm I_{IL}$	–	*	–	μA

* Value to be fixed.

CHARACTERISTICS (continued)

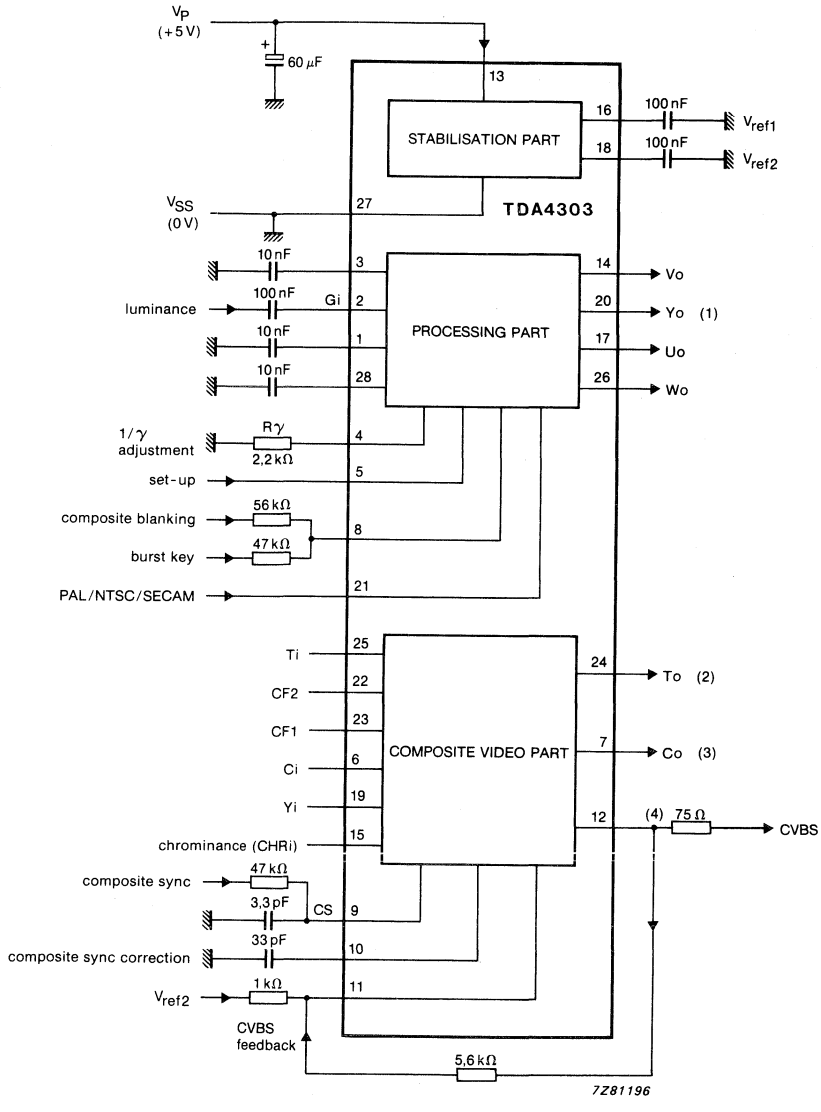
parameter	symbol	min.	typ.	max.	unit
CVBS PART (AC coupled, 150 Ω output load)					
Chrominance input (pin 15)					
DC input bias voltage = V_{ref2}					
Input voltage range (100% saturated) (peak-to-peak value)	$V_{15\text{-}27}$	–	0.5	0.55	V
Input resistance	R_{15}	100	–	–	kΩ
Input capacitance	C_I	–	–	5	pF
CVBS amplitude (pin 12)					
Black level CVBS output signal	$V_{12\text{-}27}$	–	1.6	–	V
Maximum output voltage swing (peak-to-peak value)	$V_{12\text{-}27(p\text{-}p)}$	2.7	3.6	–	V
Synchronization input pulse (CS) (peak-to-peak value)	$V_{9\text{-}27(p\text{-}p)}$	0.6	–	V_P	V
Delay between CS input to CVBS output *	t_d	200	–	–	ns
Luminance output component with Y input = 0.5 V(p-p) (peak-to-peak value)	$V_{12\text{-}27(p\text{-}p)}$	–	1.4	–	V
Chrominance output component with chrominance input = 0.6 V(p-p) (peak-to-peak value)	$V_{12\text{-}27(p\text{-}p)}$	–	2.15	–	V
Differential gain	dG	–	–	2	%
Differential phase	$d\phi$	–	–	1	deg.
Power supply rejection ratio (1 kHz) $20 \log \frac{V_{CVBS}}{V_P}$	RR	–	30	–	dB
Y input (pin 19)					
Input voltage range (peak-to-peak value)	$V_{19\text{-}27(p\text{-}p)}$	–	0.5	0.55	V
Input resistance	R19	100	–	–	kΩ
Input capacitance	C_I	–	–	5	pF

* See application information; Figs 2 and 3.

parameter	symbol	min.	typ.	max.	unit
Contour inputs (CF1 pin 23; CF2 pin 22)					
Input voltage range (peak-to-peak value)	$V_{23,22-27(p-p)}$	–	1.0	1.2	V
Contour gain range between Ci input and CVBS output	G_{6-12}	–	4.4	–	
White clipping level (with respect to 1.4 V Yo component of the CVBS output signal)		–	120	–	%
Black clipping level (with respect to 1.4 V Yo component of the CVBS output signal)		−10	−7	−5	%
WT3 buffer gain		–	2	–	
Delay between CF1 input and CVBS output	t_{d1}	–	20	–	ns
Delay between CF2 input and CVBS output	t_{d2}	–	40	–	ns

DEVELOPMENT DATA

APPLICATION INFORMATION



(1) Yo output (pin 20) = (0.587 E'G_i) – set-up.
With: E' (input amplitude) = E_i 1/γ; γ = 0.55; Rγ = 2.2 kΩ.

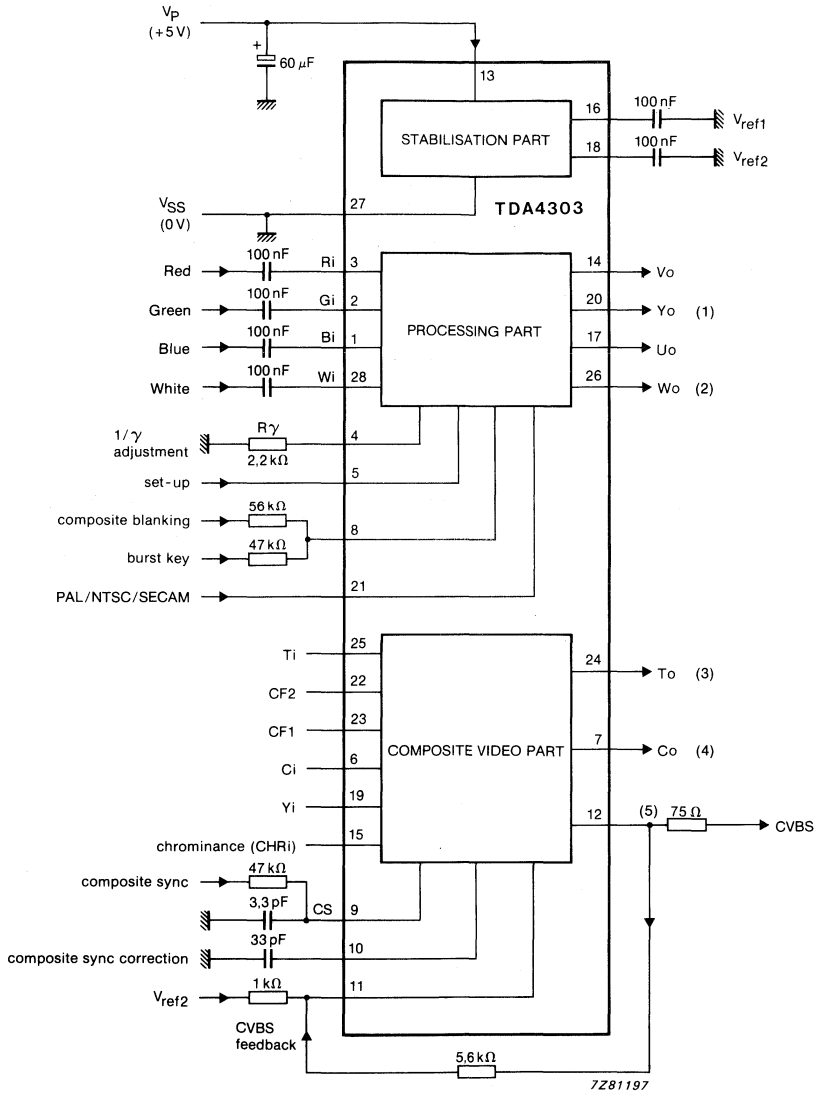
(2) To output (pin 24) = 2 x Ti.
(input Ti biassed to V_{ref2} when not used).

(3) Co output (pin 7) = 2 x (CF2 – CF1).
(inputs CF1, CF2 biassed to V_{ref2} when not used).

(4) CVBS output (pin 12) = (1.4 CF2 + 4.4 Ci + 2.8 Yi + 3.58 CHRi) – 0.615 CS
(inputs CF2, Ci, Yi, CHRi, CS biassed to V_{ref2} when not used).

Fig.2 Application diagram for black and white television camera.

DEVELOPMENT DATA



(1) Yo output (pin 20) = (Y − Wo) − set-up.
With: Y = 0.299 E_iRi + 0.587 E'Gi + 0.114 E'Bi and
E' (input amplitude) = E_i 1/γ; γ = 0.55; Rγ = 2.2 kΩ.

(2) Wo output (pin 26) = Wi.

(3) To output (pin 24) = 2 x Ti.
(input Ti biassed to V_{ref2} when not used).

(4) Co output (pin 7) = 2 x (CF2 − CF1).
(inputs CF1, CF2 biassed to V_{ref2} when not used).

(5) CVBS output (pin 12) = (1.4 CF2 + 4.4 Ci + 2.8 Yi + 3.58 CHRi) − 0.615 CS
(inputs CF2, Ci, Yi, CHRi, CS biassed to V_{ref2} when not used).

Fig.3 Application diagram for colour television camera.

MASTER GAIN

GENERAL DESCRIPTION

The TDA4306 is an integrated circuit which controls the amplification of the four output signals (White, Yellow, Green and Cyan) from the frame transfer sensors (NXA1021 to NXA1041). The matching of the four channels is excellent over the whole control and temperature range. An on-chip white clipping circuit protects the white processor (TDA4303) from output signals that are too large. If white clipping occurs, a pulse is available to kill the colour information. Highlights will always be white, not coloured.

Features

- Four variable gain amplifiers
- White clipping circuit
- Blanking switch
- 2.1 V reference voltage

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 20)	$V_P = V_{20\text{-}10}$	4.75	5.0	5.25	V
Reference voltage (pin 6)	V_{ref}	1.9	2.1	2.3	V
Total power dissipation	P_{tot}	90	140	200	mW
Storage temperature range	T_{stg}	−25	–	+ 150	°C
Operating ambient temperature range	T_{amb}	−20	–	+ 70	°C

PACKAGE OUTLINES

TDA4306 : 20-lead DIL; plastic (SOT146).
TDA4306T: 20-lead mini-pack; plastic (SO20; SOT163A).

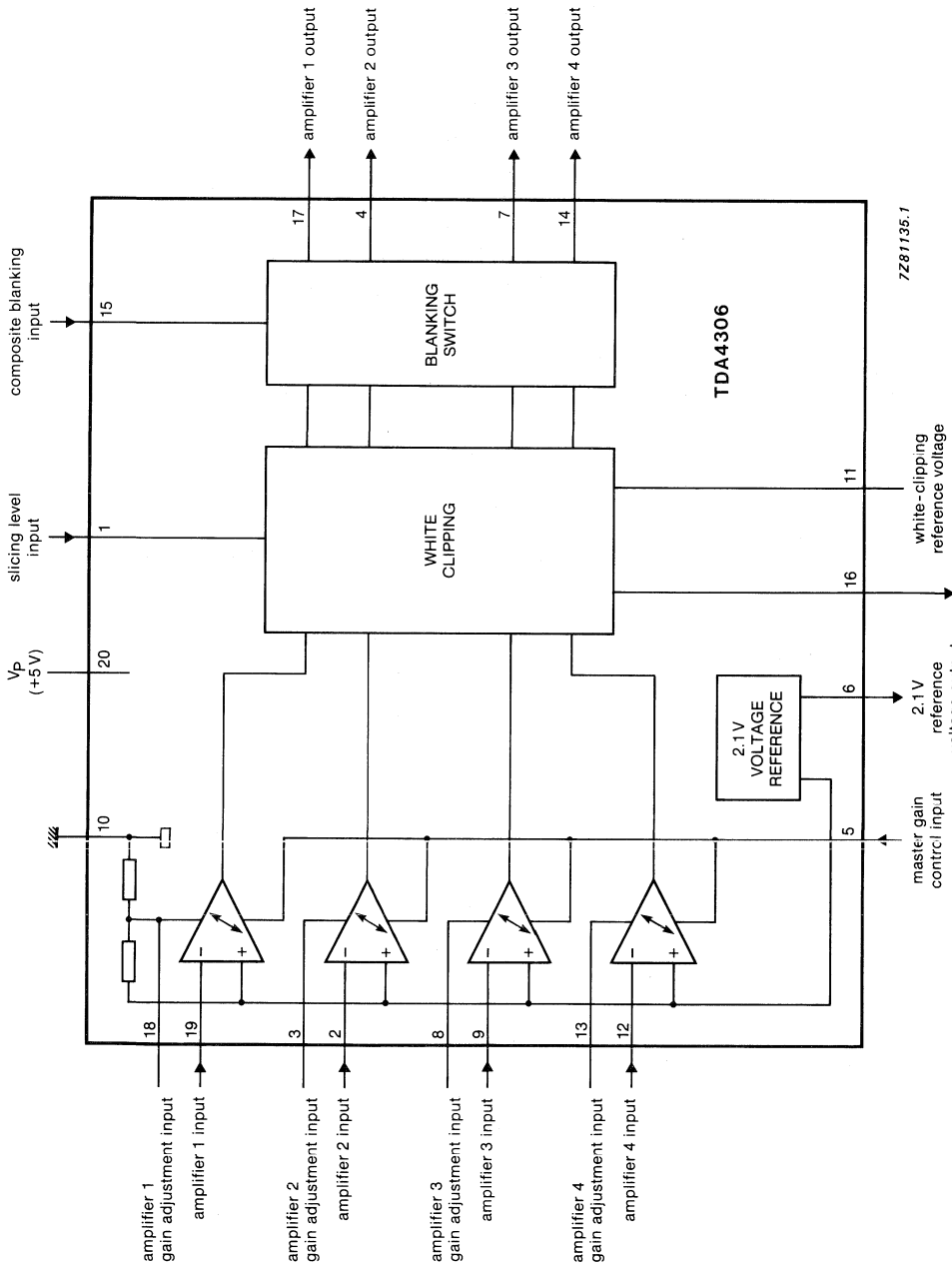


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage (pin 20)	V_P	–	12	V
Input voltage (pins 1, 2, 3, 5, 8, 9 12, 13, 15, 18 and 19)	V_I	–	5	V
Output current (pins 17, 4, 7 and 14) $t < 1$ s	I_O	–	100	mA
Total power dissipation				
SO package*	P_{tot}	–	370	mW
DIL package	P_{tot}	–	1000	mW
Operating ambient temperature range	T_{amb}	–20	+ 70	°C
Storage temperature range	T_{stg}	–25	+ 150	°C

DEVELOPMENT DATA

* Mounted on a printed-circuit board.

CHARACTERISTICS

$V_P = V_{20-10} = 5$ V; $T_{amb} = 25\,^{o}C$ unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (pin 20)	V_P	4.75	5.0	5.25	V
Reference voltage (pin 6)	V_{ref}	1.9	2.1	2.3	V
Temperature drift of V_{ref}	ΔV_{ref}	–	0.18	–	mV/°C
External load current	$I_{L(ext.)}$	–	–	10	mA
Total power dissipation	P_{tot}	90	140	200	mW
Variable gain amplifiers					
Inputs (pins 2, 9, 12 and 19; note 1)					
Input voltage (peak-to-peak value)					
negative video	$V_{n-10(p-p)}$	–	–	–1100	mV
positive video (gain = 1)	$V_{n-10(p-p)}$	–	–	400	mV
Input bias current at $V_I = 2.6$ V	$I_{n(bias)}$	–	2.2	5	μA
Input resistance	$R_{2, 9, 12, 19}$	–	300	–	kΩ
Outputs (pins 17, 4, 7 and 14)					
DC offset voltage of input to output (output = V_{ref})		–	–	–220	mV
DC offset voltage of input to output (output = V_{ref})		–	–	100	mV
Offset voltage between blanked output and V_{ref}		–	–	2	mV
Drift of blanked output voltages	ΔV_O	10	–	–	μV/°C
Output sink current	I_{OS}	–	–	100	μA
Resistive load of output to ground	R_L	1.5	–	–	kΩ
Output voltage swing at $V_{ref} = 2.1$ V		–	V_{ref}–500 mV	–	
Output voltage swing at $V_{ref} = 2.1$ V		–	V_{ref}+ 1200 mV	–	
Output impedance	$\|Z_O\|$	–	100	–	Ω
Power supply rejection ratio (1 kHz)	RR	–	30	–	dB
Bandwidth	B	6	–	–	MHz

parameter	symbol	min.	typ.	max.	unit
Master gain control input (pin 5)					
Gain control range			see Fig. 2		
Input current at V_{5-10} = 0 V	I_5	–	–	30	μA
Matching of gain (note 2) between the 4 channels ($f_{temp.\ range}$ and as $f_{gain\ range\ 2\ to\ x\ 8}$)		–	–	1	%
Gain stability = $f_{temp.range}$ $-20 < t < 60$ °C		–	3	–	%
Differential gain	dG	–	–	1	%
Differential phase	dφ	–	–	2	deg.
Gain adjustment inputs (pins 18, 3, 8, 13)					
Input voltage range	V_{adj}	0.9	–	1.9	V
Overall gain (MG = 2)					
at V_{adj} = 0.9 V	G	–	–	2.2	
at V_{adj} = 1.9 V	G	1.5	–	–	
Input current (pins 3, 8 and 13) at V_I = 1,6 V	I_I	–	–	2	μA
Input resistance (pin 18)	R_{18}	–	3.25	–	kΩ
Input voltage (pin 18; open-circuit)	V_I	–	1.2	–	V
White clipping circuit					
Slicing level (pin 1)					
input voltage range	V_{1-10}	0.5	–	1.8	V
input current at V_{1-10} = 1 V	I_1	–	–	2	μA
White clipping reference voltage (pin 11)	V_{11-10}	–	V_{1-10} x 2.5 V	–	V
Output pulse (pin 16) (peak-to-peak value)	$V_{16-10(p-p)}$	3.0	–	–	V
Output voltage (pin 16)					
LOW	V_{OL}	–	–	1	V
HIGH	V_{OH}	4	–	–	V
Output sink current (pin 16)	I_{OS}	–	–	0.1	mA
Delay of a variable gain amplifier input to white clipping output	t_d	–	–	100	ns

DEVELOPMENT DATA

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Blanking switch (pin 15)					
Composite blanking input voltage					
active HIGH	V_{15-10}	2.4	–	V_P	V
active LOW	V_{15-10}	–	–	1.4	V
Input current at $V_{15-10} = 5$ V	I_{15}	–	–	2	μA
Input capacitance	C_I	–	–	5	pF
Delay between blanking input and one of the 4 amplifier outputs	t_d	–	40	100	ns

Notes to the characteristics

1. The maximum input voltage is permitted only if the input voltage minus the DC offset voltage = 2.1 V. If the input voltage minus the DC offset voltage = 1.6 V, the maximum input voltage is 1 V(p-p).
2. Over the range 2 to x 8, after that each channel is adjusted to 0. This is possible only if the blanking pulse is switched off and the DC input voltage is equal to V_{ref}.

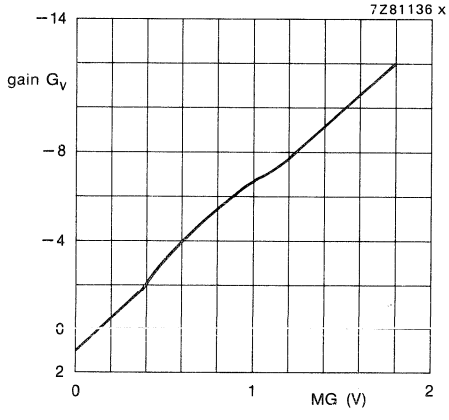
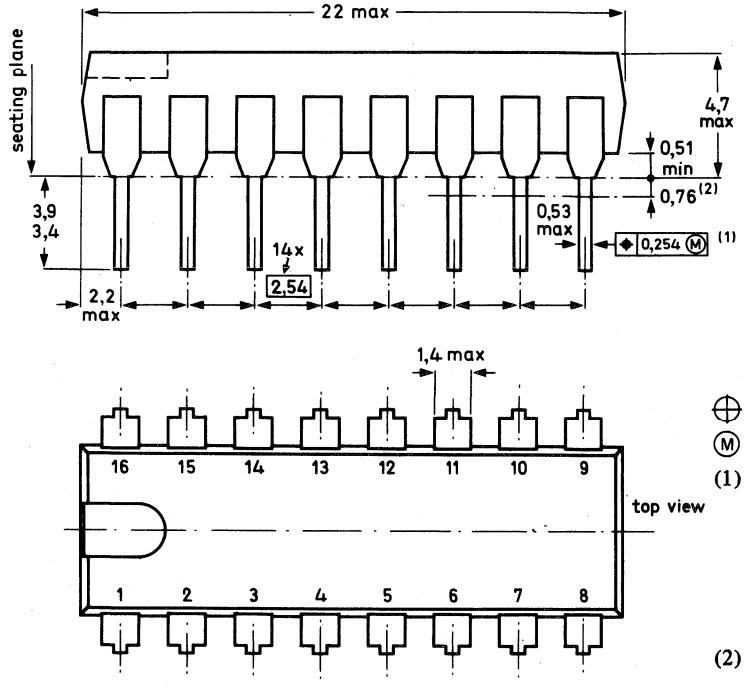


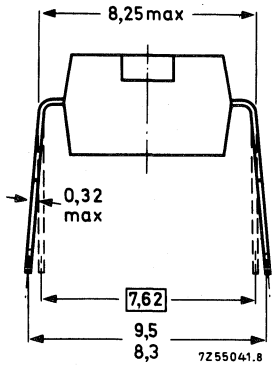
Fig.2 Gain as a function of V_{MG}.

PACKAGE INFORMATION

Package outlines
Soldering

16-LEAD DUAL IN-LINE; PLASTIC (SOT38)





Dimensions in mm

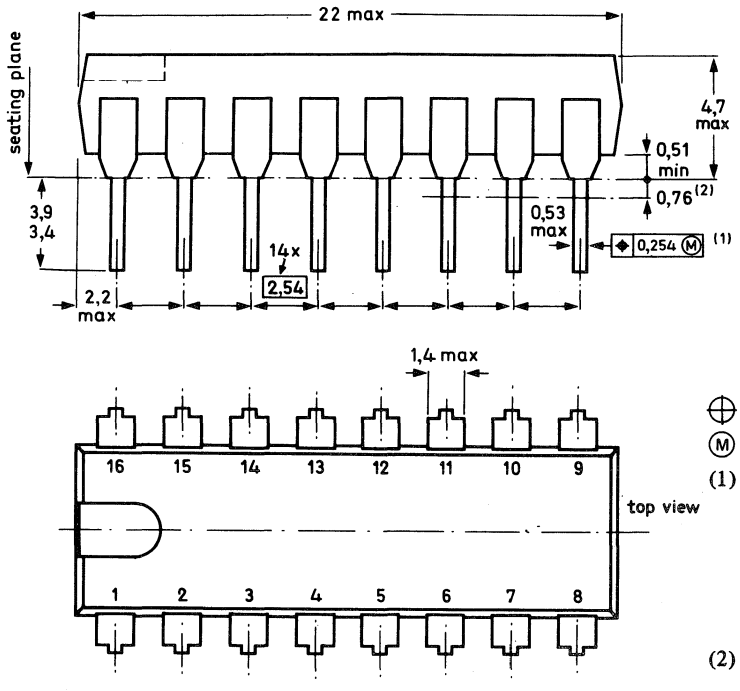
⊕ Positional accuracy.

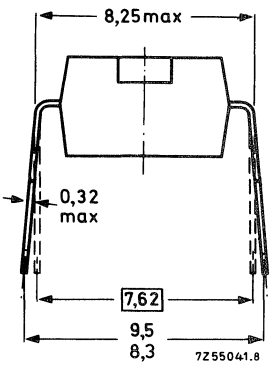
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

16-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT38)





Dimensions in mm

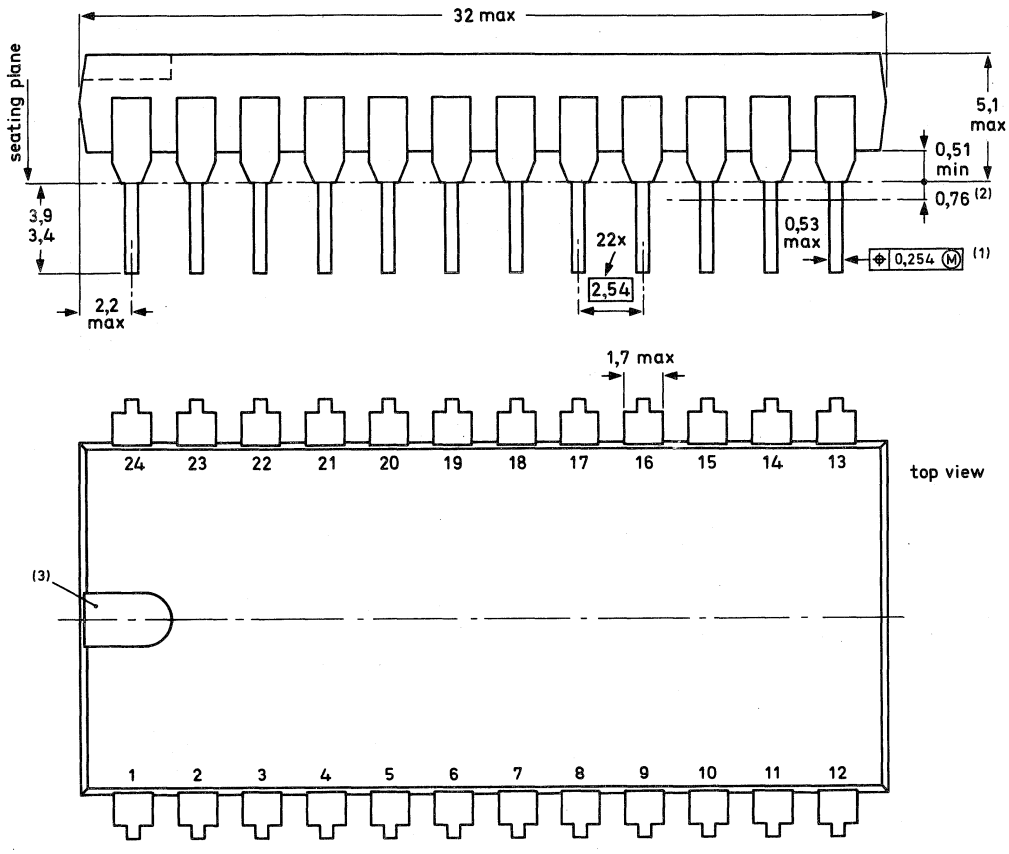
⊕ Positional accuracy.

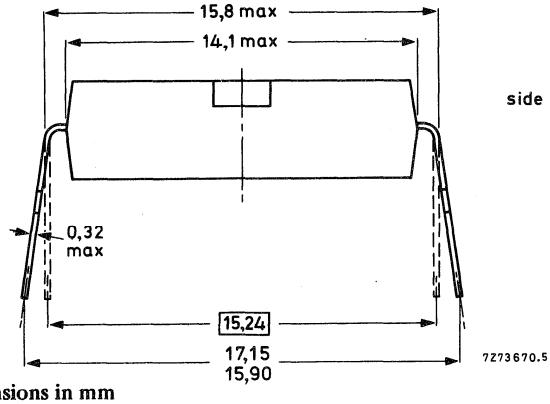
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

24-LEAD DUAL IN-LINE; PLASTIC (SOT101A, B, F, G, L)





Dimensions in mm

⊕ Positional accuracy.

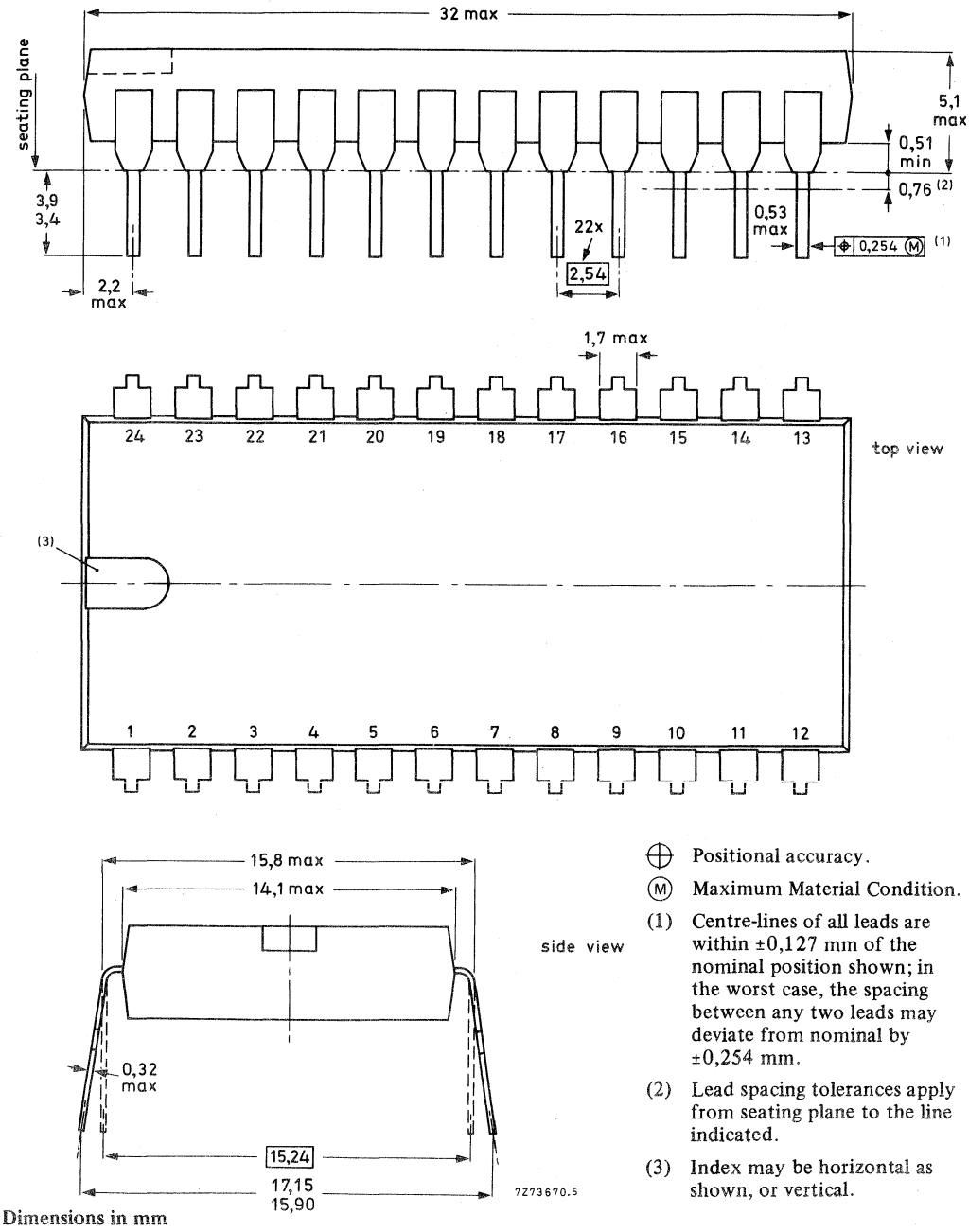
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

24-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT101A, B, F, G, L)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

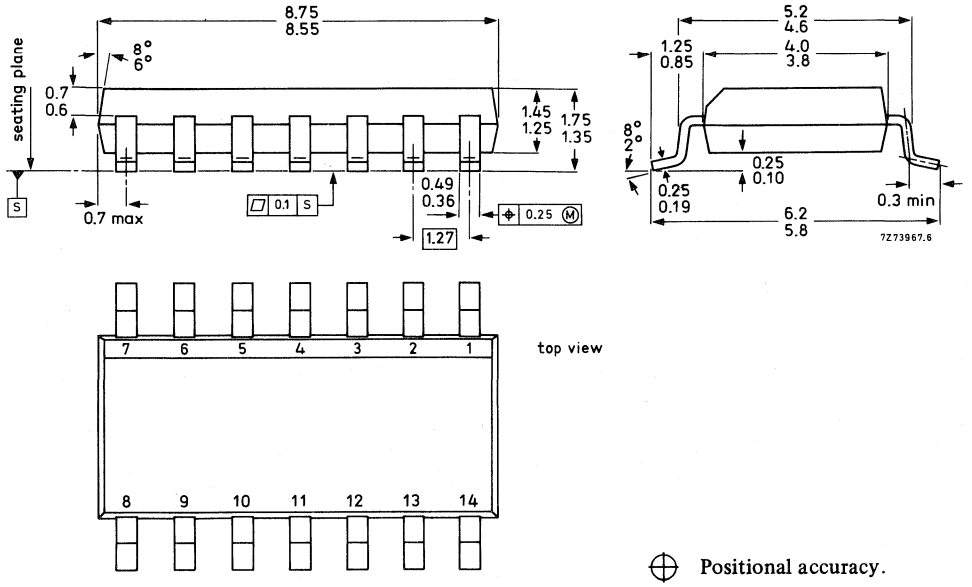
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

14-LEAD MINI-PACK; PLASTIC (SO14; SOT108A)

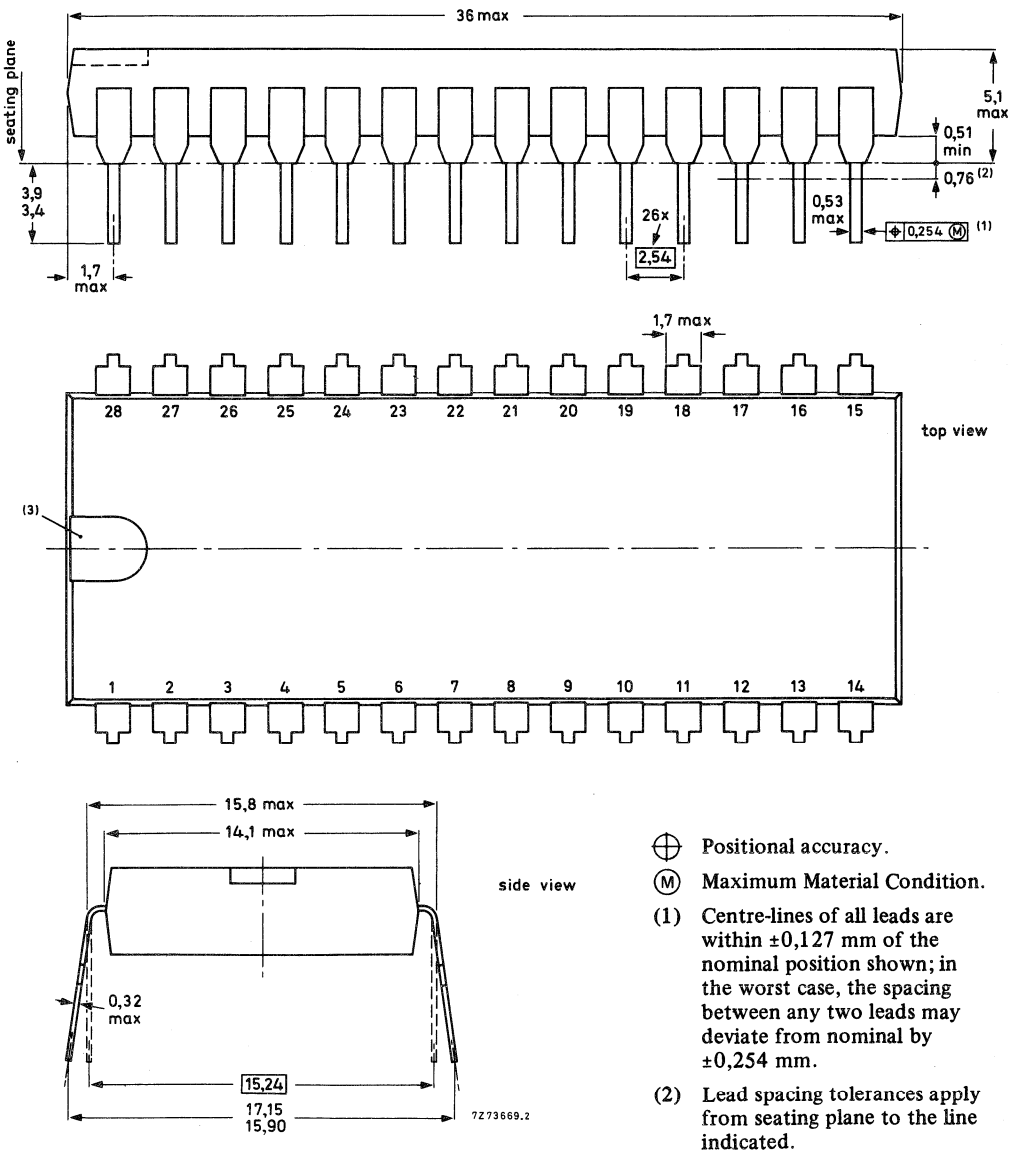


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimension in mm

28-LEAD DUAL IN-LINE; PLASTIC (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

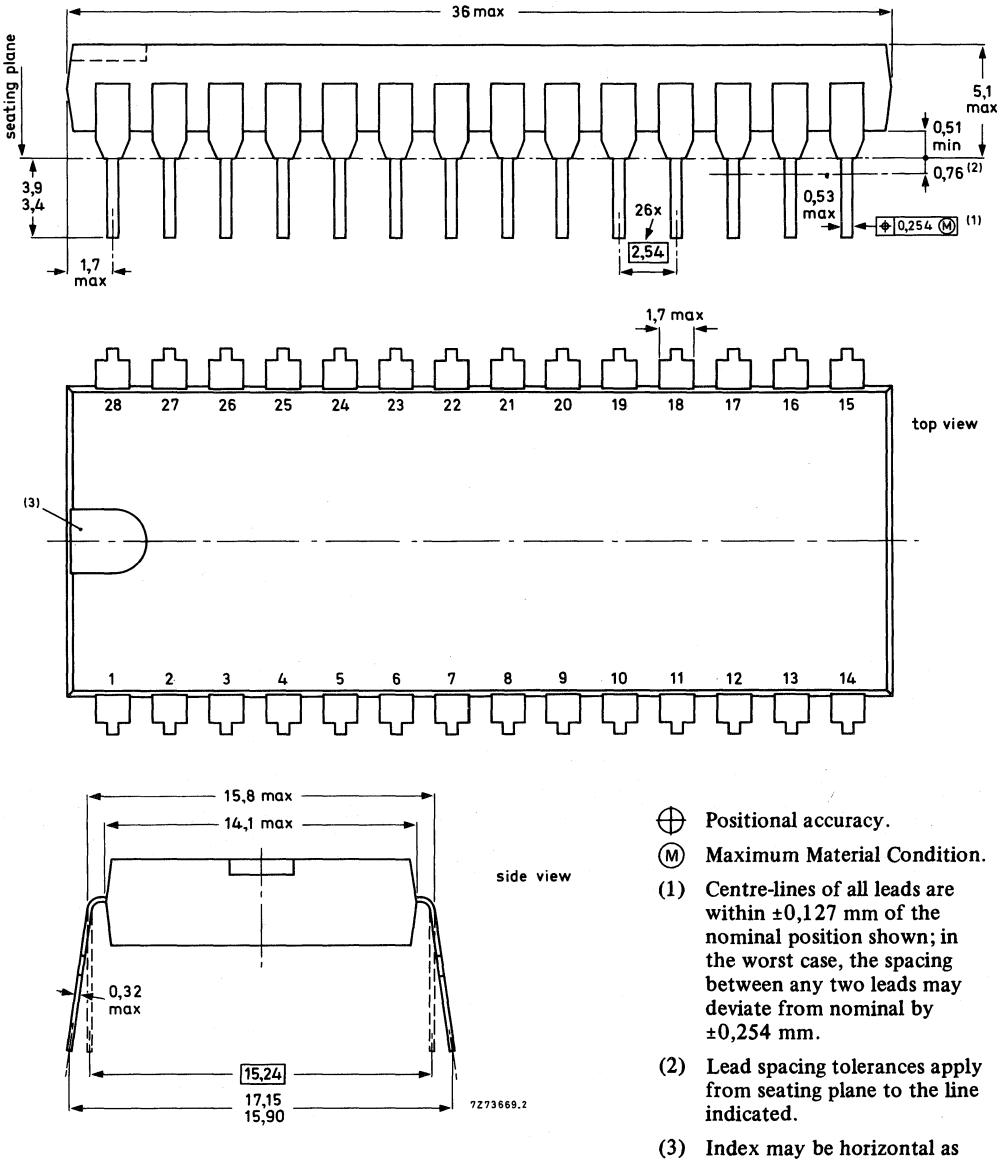
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC WITH INTERNAL HEAT SPREADER (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

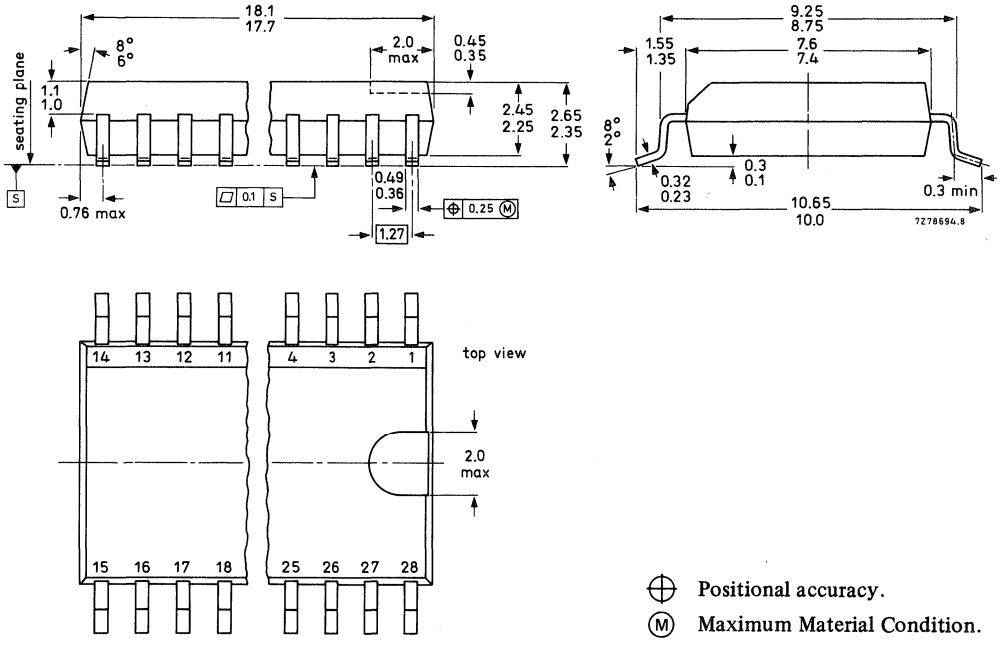
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

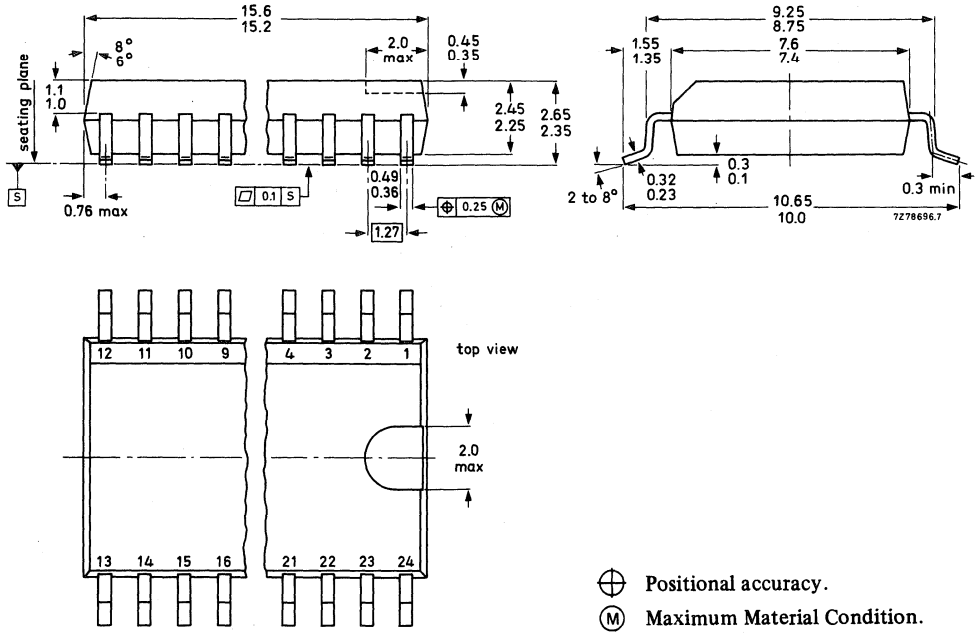
Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO28; SOT136A)



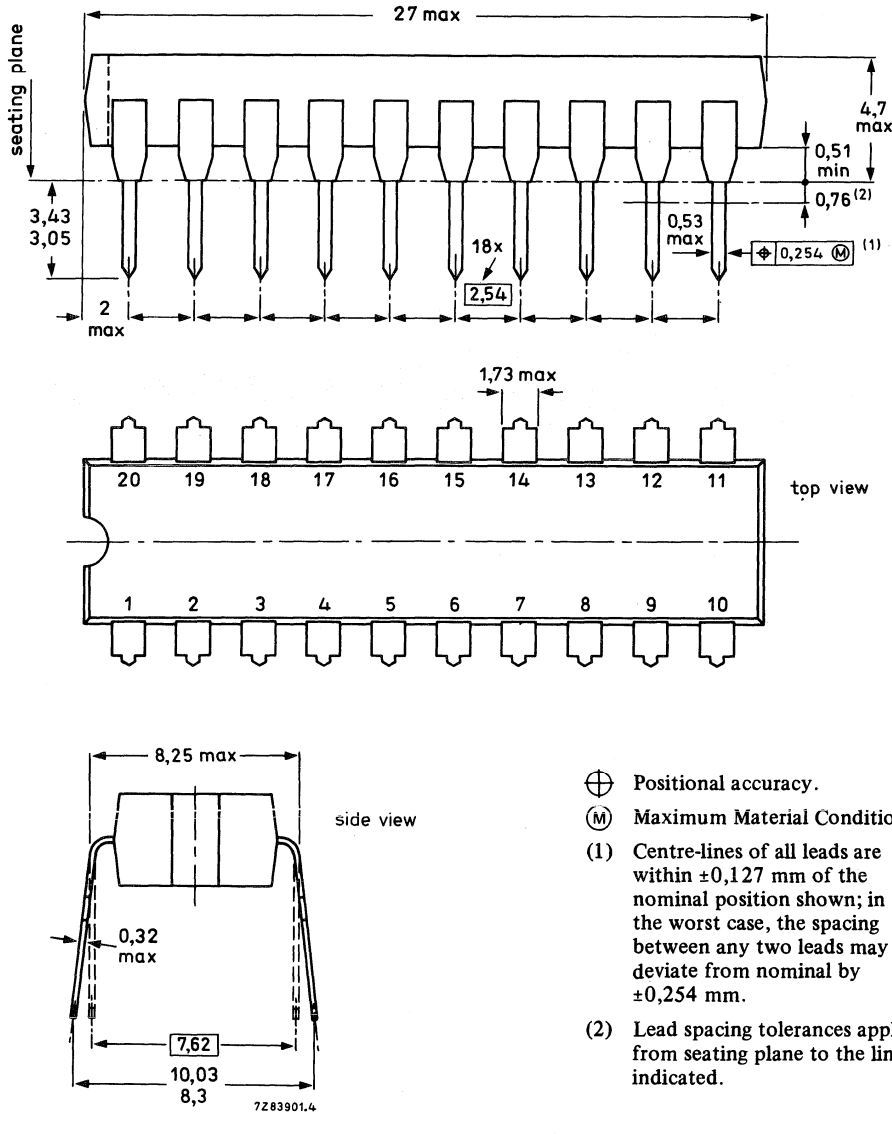
Dimensions in mm

24-LEAD MINI-PACK; PLASTIC (SO24; SOT137A)



Dimensions in mm

20-LEAD DUAL IN-LINE; PLASTIC (SOT146)



⊕ Positional accuracy.

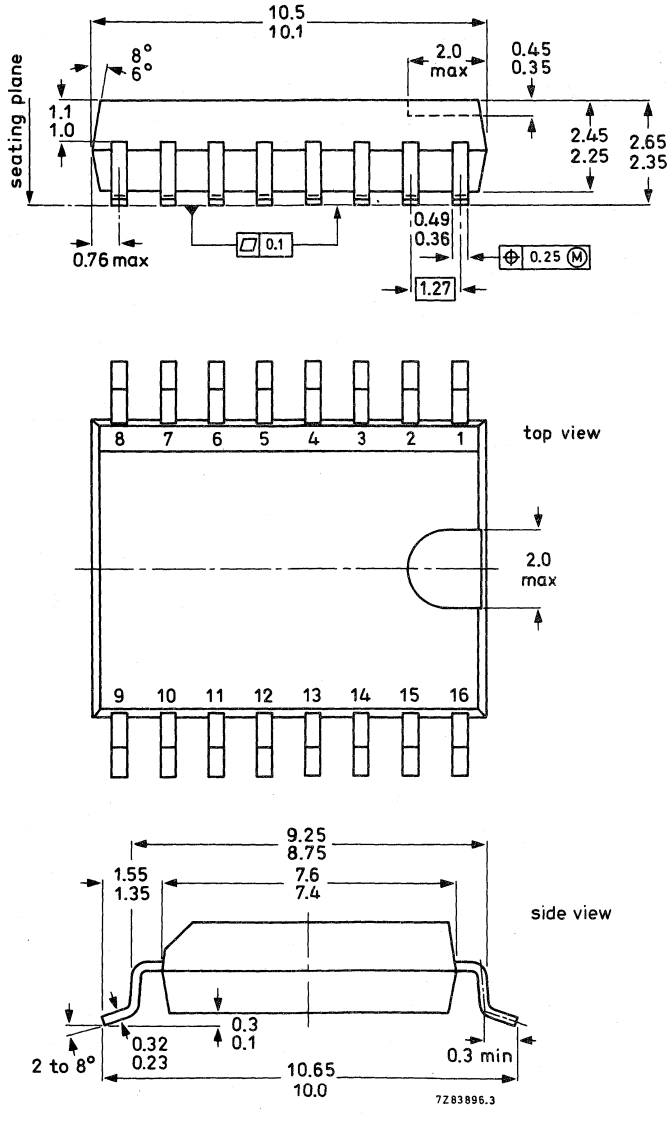
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16L; SOT162A)

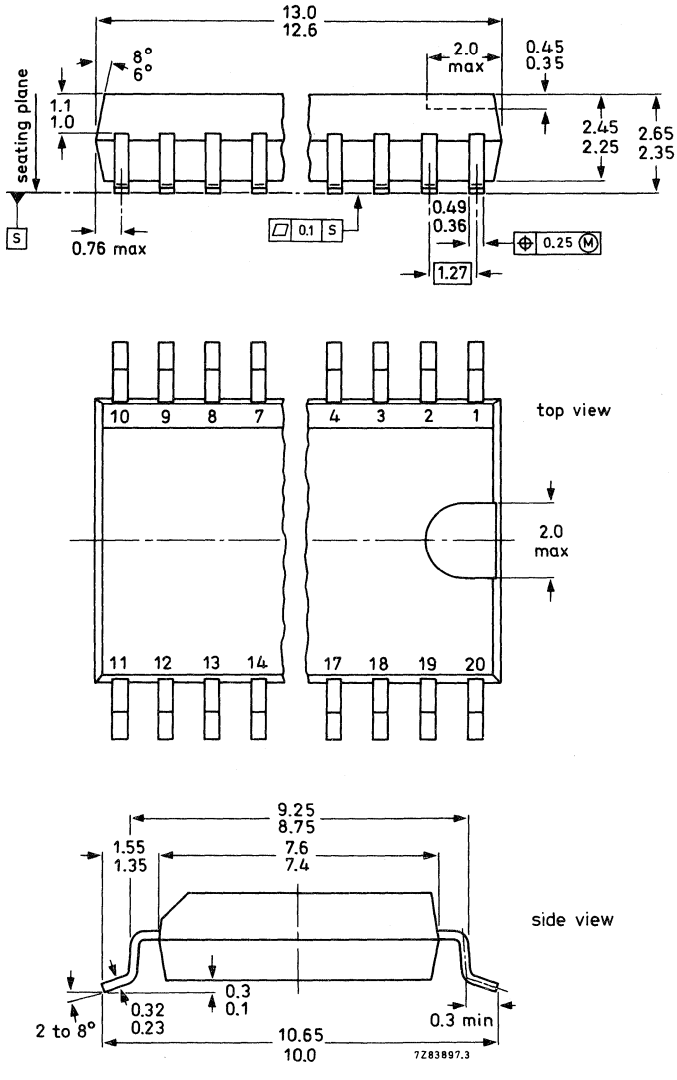


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

20-LEAD MINI-PACK; PLASTIC (SO20; SOT163A)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

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DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of six series of handbooks:

INTEGRATED CIRCUITS

DISCRETE SEMICONDUCTORS

DISPLAY COMPONENTS

PASSIVE COMPONENTS*

PROFESSIONAL COMPONENTS**

MATERIALS*

The contents of each series are listed on pages iii to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Components is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Components and materials (green) series of handbooks.
** Will replace the Electron tubes (blue) series of handbooks.

INTEGRATED CIRCUITS

This series of handbooks comprises:

code	handbook title
IC01	**Radio, audio and associated systems** Bipolar, MOS
IC02a/b	**Video and associated systems** Bipolar, MOS
IC03	**ICs for Telecom** Bipolar, MOS Subscriber sets, Cordless Telephones
IC04	**HE4000B logic family** CMOS
IC05	**not yet issued**
IC06	**High-speed CMOS; PC74HC/HCT/HCU** Logic family
IC07	**Advanced CMOS logic (ACL)**
IC08	**ECL 10K and 100K logic families**
IC09N	**TTL logic series**
IC10	**Memories** MOS, TTL, ECL
IC11	**Linear Products**
Supplement to IC11	**Linear Products**
IC12	**I^2C-bus compatible ICs**
IC13	**Semi-custom** Programmable Logic Devices (PLD)
IC14	**Microcontrollers** NMOS, CMOS
IC15	**FAST TTL logic series**
IC16	**CMOS integrated circuits for clocks and watches**
IC17	**ICs for Telecom** Bipolar, MOS Radio pagers Mobile telephones ISDN
IC18	**Microprocessors and peripherals**
IC19	**Data communication products**

DISCRETE SEMICONDUCTORS

This series of data handbooks comprises:

current code	new code	handbook title
S1	**SC01**	**Diodes** High-voltage tripler units
S2a	**SC02***	**Power diodes**
S2b	**SC03***	**Thyristors and triacs**
S3	**SC04***	**Small-signal transistors**
S4a	**SC05**	**Low-frequency power transistors and hybrid IC power modules**
S4b	**SC06**	**High-voltage and switching power transistors**
S5	**SC07***	**Small-signal field-effect transistors**
S6	**SC08***	**RF power transistors**
	SC09	**RF power modules**
S7	**SC10**	**Surface mounted semiconductors**
S8a	**SC11***	**Light emitting diodes**
S8b	**SC12**	**Optocouplers**
S9	**SC13***	**PowerMOS transistors**
S10	**SC14***	**Wideband transistors and wideband hybrid IC modules**
S11	**SC15**	**Microwave transistors**
S15**	**SC16**	**Laser diodes**
S13	**SC17**	**Semiconductor sensors**
S14	**SC18***	**Liquid crystal displays and driver ICs for LCDs**

* Not yet issued with the new code in this series of handbooks.
** New handbook in this series; will be issued shortly.

DISPLAY COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T8	DC01	**Colour display systems**
T16	DC02*	**Monochrome tubes and deflection units**
C2	DC03*	**Television tuners, coaxial aerial input assemblies**
C3	DC04*	**Loudspeakers**
C20	DC05*	**Wire-wound components for TVs and monitors**

* These handbooks are currently issued in another series; they are not yet issued in the Display Components series of handbooks.

PASSIVE COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
C14	PA01	**Electrolytic capacitors; solid and non-solid**
C11	PA02*	**Varistors, thermistors and sensors**
C12	PA03*	**Potentiometers, encoders and switches**
C7	PA04*	**Variable capacitors**
C22	PA05*	**Film capacitors**
C15	PA06*	**Ceramic capacitors**
C9	PA07*	**Piezoelectric quartz devices**
C13	PA08*	**Fixed resistors**

* Not yet issued with the new code in this series of handbooks.

PROFESSIONAL COMPONENTS

This series of data handbooks comprises:

current code	new code	handbook title
T1	*	Power tubes for RF heating and communications
T2a	*	Transmitting tubes for communications, glass types
T2b	*	Transmitting tubes for communications, ceramic types
T3	PC01**	High-power klystrons
T4	*	Magnetrons for microwave heating
T5	PC02**	Cathode-ray tubes
T6	PC03**	Geiger-Müller tubes
T9	PC04**	Photo and electron multipliers
T10	PC05**	Plumbicon camera tubes and accessories
T11	PC06	Microwave diodes and sub-assemblies
T12	PC07	Vidicon and Newvicon camera tubes and deflection units
T13	PC08	Image intensifiers
T15	PC09**	Dry reed switches
C8	PC10	Variable mains transformers; annular fixed transformers
	PC11	Solid state image sensors and peripheral integrated circuits

* These handbooks will not be reissued.
** Not yet issued with the new code in this series of handbooks.

MATERIALS

This series of data handbooks comprises:

current code	new code	handbook title
C4 } C5 }	MA01*	**Soft Ferrites**
C16	MA02**	**Permanent magnet materials**
C19	MA03**	**Piezoelectric ceramics**

* Handbooks C4 and C5 will be reissued as one handbook having the new code MA01.

** Not yet issued with the new code in this series of handbooks.

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